THE MODELING AND MEASUREMENT OF PARASITIC AND EQUIVALENT CIRCUIT ELEMENTS IN VERTICAL AND LATERAL BIPOLAR JUNCTION TRANSISTORS

By

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Abstract of Dissertation Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy

THE MODELING AND MEASUREMENT OF PARASITIC AND EQUIVALENT CIRCUIT ELEMENTS IN VERTICAL AND LATERAL BIPOLAR JUNCTION TRANSISTORS

BY

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This dissertation presents the characterization and modeling of the passive and active elements of bipolar VLSI circuits. For the passive elements, the contact pads and interconnects are characterized by interpreting s-parameter measurements. A new three-step de-embedding method is developed to correct for the environment of the device under test (DUT) and extract its characteristic s-parameters. In this de-embedding method, the correction includes subtracting the series parastics as well as the shunt parasitics of the pads and interconnects from the DUT. For npn transistors, the base impedance, which includes the dc and ac crowding effect in the emitter-base junction, is measured and characterized using this de-embedding approach. The experimental data of base

impedance, both lumped and distributed, are extracted from the s-parameter measurement and compared with a previously existing model for the npn transistor.

A charge-based semi-numerical model for the lateral pnp transistor is developed for dc, ac and transient conditions. This model simplifies the two-dimensional current flow into two parts by deriving the analytical geometrical factors. The transient and small-signal models are developed from the dc model by evaluating derivatives of charges and currents about junction voltages. The substrate p-n-n^+—p transistor, which is a parasitic transistor in the lateral pnp transistor, is modeled and incorporated into the lateral pnp BJT model. This developed lateral pnp transistor model is implemented in SPICE (LMSPICE).

CHAPTER 1
INTRODUCTION

The ongoing process of shrinking the dimensions of the bipolar junction transistor (BJT), which is increasing the device speed and improving the integration level, results in several previously neglected phenomena becoming more important in integrated circuit design. The effects which have been neglected in the past include the parastics of contact pads and interconnects, the various distributed crowding effects (dc, ac and transient crowding effects) in the emitter-base regions of the vertical npn transistor and the lateral pnp transistor in bipolar VLSI circuits. The purpose of this dissertation is to characterize the parasitic passive and active elements of bipolar VLSI circuits.

At high frequencies, the power consumed by the contact pads and interconnects is comparable to that of the device itself. Therefore, it is very important to calibrate and correct or de-embed the measured data of the device under test (DUT) from the contact pad and interconnect environment. A new three-step de-embedding method is developed to correct for the environment of the DUT.

For modern devices which have extremely narrow base widths and which operate at high current densities and frequencies,

ac emitter crowding effects, accentuated by dc crowding, are very important in the device performance. Therefore, it is critical to model these phenomena and incorporate them into the existing model for efficient and precise computer-aided circuit design (CAD). The base impedance, which includes the dc and ac crowding effects, is measured. New extraction methods, using the s-parameter measurement and de-embedding procedure, are developed and compared with an existing model [JO91].

In many circuit applications, the lateral pnp transistor is widely used as a complementary transistor to the vertical npn because of compatible fabrication steps. In Fig. 1.1, a cross section of a lateral pnp transistor is given. The base region of the device is formed by the n-type epitaxial layer which serves as the collector of the npn transistor. The p-type base diffusion of the npn transistor is used to form the emitter and the collector regions of the lateral pnp transistor. The n^+-type emitter diffusion of the npn transistor is used to form the n^+-type contact region for the pnp device. The pnp transistor action takes place in the lateral direction, hence the name lateral pnp. Because of design tolerances, the minimum base width is of the order of the epitaxial layer thickness. This value is much larger than that of the process-compatible vertical npn transistor. Thus, the current gain and the frequency performance of the lateral

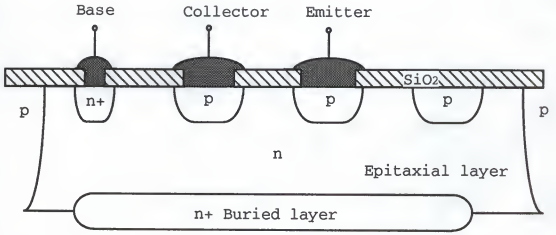


Figure 1.1 The cross section of a lateral pnp transistor.

pnp transistors are inferior to those of the npn devices. The inferiority of the lateral pnp transistor's performance can be a deciding limitation on the performance of complementary bipolar integrated circuit. For a proper circuit design, a predictive circuit-level model for the lateral pnp transistor is essential. A semi-numerical, CPU-efficient model for the lateral pnp transistor is herein developed for dc, small-signal and transient conditions. The dc model includes

(1) a lateral current flowing from the emitter to the collector sidewall and a more vertical flow along the curved trajectory between the emitter and collector junction bottoms,

(2) the parasitic substrate transistor formed by the emitter, the epitaxial base region, the buried layer and the substrate (p-n-n^+-p) and

(3) high-level injection in the base region: since the base region is a lightly doped n-type epitaxial layer, high-level injection occurs at a much lower collector current than in the vertical npn transistor.

In the large-signal and small-signal models, the charge of each region is the fundamental variable and the model definition is similar in type to charge-based models for the vertical npn [JE089, J091]. The models are implemented in the SPICE2 code.

In Chapter 2, the s-parameter measurements and a new de-embedding method are presented. The s-parameters or

scattering parameters relate those electromagnetic waves scattered (or reflected) from the network or device-under-test to those waves incident upon the network. It is the high-frequency analog to the y-parameter measurement which is a function of the voltage and current characteristics of the device with a short or open at the other port. Because both measurements are two-port measurements, the s-parameters can be converted to y- (or h-) parameters and vice versa [HPAPP]. Recent developments in high-frequency measurement instrumentation, such as the HP 8510 Automated Network Analyzer (ANA) and the Cascade Microtek probes, have greatly improved the flexibility and accuracy of microwave characterization. As the dimension of the BJT shrinks and its speed increases, an accurate procedure is needed to de-embed the DUT from its environment, i.e., contact pad and interconnect parastics. Since the contact pad and interconnect parastics are not reduced concomitantly with the transistor scale, the calibration and de-embedding technique of the DUT are critical to interpreting its s-parameter measurements. We developed a new de-embedding method which includes subtracting the series parasitics from the DUT as well as the shunt elements that are normally subtracted out. The series parasitics are shown to be especially important to understanding the BJT high frequency operation. An existing quasi-static multi-regional charge-based model [JO91] shows

good agreement with this interpreted measurement data using the new de-embedding method.

In Chapter 3, the base impedance of the vertical npn is extracted from s-parameter measurements. The vertical BJT has several complex crowding mechanisms which are not properly modeled. One of these affects is the base impedance, which can be a major element in the delay of the device and is a function of bias and small and large-signal operating conditions. Several authors [Hau64, Lar85, JO90] have developed dc models for base resistance which include the effects of emitter debiasing or emitter crowding. Ghosh [GHO65] pointed out that base resistance should be replaced by a base impedance to account for the ac crowding effects in the high frequency region. Since advanced BJTs have high operating frequencies and current densities and, therefore, they are fast enough to incur ac crowding effects, a compact model for base impedance is needed for proper ac modeling. Herein, the base impedance is extracted from s-parameter measurement and two new methods for interpreting base impedance are developed. One new method includes the effect of the base-collector capacitance (c_{μ}) and the other includes the effect of the peripheral transistor. This base impedance model will be incorporated into our multi-regional model in the future.

In Chapter 4, a new large-signal model for the lateral pnp transistor including its parasitic substrate transistor

is verified by comparing simulations with dc, transient and ac measurements. The charge-based semi-numerical model is predictive. The critical inputs into the model depend on dopant profiles and layout geometries. Since the base width of typical lateral pnp's is wide, non-quasi-static (NQS) effects can be important in the transient and ac modeling. We adopt an existing method of partitioning the base charge between the emitter and collector junctions [FOS86] which accounts for NQS effects to first order in transient and small-signal simulations.

In Chapter 5, the main accomplishments of this dissertation are summarized and obvious directions for further research are discussed.

In the Appendix, the method for the implementation of the lateral pnp transistor model into SPICE2 is given.

CHAPTER 2
A THREE-STEP METHOD FOR THE DE-EMBEDDING OF HIGH FREQUENCY S-PARAMETER MEASUREMENTS

2.1 Introduction

In device modeling and small-signal model verification for circuit simulation, some of the device parameters are extracted from experimental data taken at high frequencies (45 MHz to 26.5 GHz) using s- (scattering-) parameters. S-parameters are being used more and more in microwave design because they are more suitable for high frequency measurement than other parameters. Other two-port parameters need the input and output of the device to be open and short-circuited, which is difficult to do at radio frequencies and above because of the parasitic inductance and capacitance in the shorts and opens. S-parameters, on the other hand, are measured with the device embedded between a 50Ω load and source and there is not much chance for oscillation to occur. Therefore, the s-parameters can be used for investigating the frequency response of advanced devices at high frequencies. The definition of s-parameters are

$$s_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad s_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$
$$s_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \qquad s_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2.1}$$

where a_i and b_i are normalized complex voltage waves incident on and reflected from the i^{th} port of the network. From the above definition, one can see that s_{11} represents the input reflection coefficient with the output port terminated by a matched load. ($Z_L = Z_0$ sets $a_2 = 0.$) S_{22} represents the output reflection coefficient with the input port terminated by a matched load. ($Z_S = Z_0$ and $V_s = 0$ set $a_1 = 0.$) S_{21} represents the forward transmission (insertion) gain with the output port terminated by a matched load. S_{12} represents the reverse transmission (insertion) gain with the input port terminated by a matched load.

Typical device parameters extracted from s-parameter measurements and/or optimized for advanced digital and analog silicon bipolar junction transistors (BJTs) are the unity-gain frequency and its inverse time constants [BEI86], the intrinsic base resistance [LAR85], and parasitic transistor elements such as the extrinsic base-collector capacitance [WIJ88]. The HP-8510 Automated Network Analyzer (ANA) and Cascade Microtek probes make it possible to measure s-parameters up to 26.5 GHz, which is above the cutoff frequency of most advanced silicon BJTs. (For example, the f_T in [CHE89] is given as 26.26 GHz and is the highest f_T so far reported for silicon BJTs.) Higher BJT frequency response is typically achieved by scaling down the lateral as well as vertical transistor dimensions [HAM88] which then results in

a reduction in the size of the parasitic transistor elements. However, for high frequency measurement, the probe pad and interconnect configuration is typically not significantly scaled. Because of the continuous reduction in the transistor dimensions without a concomitant reduction in the probe pad or interconnect size, the probe pad and interconnect parasitics need to be accurately subtracted out, that is, de-embedded from (or calibrated relative to), the measured data in to obtain the correct device s- (h- and y-) parameters.

There are several techniques for de-embedding the device-under-test (i.e., this is the BJT including the pad and interconnects and is abbreviated DUT) thereby calibrating the s-parameter measurements [FRA88, WIJ87]. Cascade Microtek provides a calibration (ISS) substrate with its probes which can be used to extend the reference plane to the probe tips. While accurate for larger transistor structures, this technique alone is not sufficient for accurately measuring advanced BJTs with emitter window dimensions $< 2 \times 8\ \mu m^2$. The s-parameters of on-wafer standards consisting of an open, two shorts, a thru, and a 50-Ω load can be subtracted from the DUT measurements automatically using the HP 8510. However, the HP 8510 is programmed to assume that the open is perfect and not lossy. This is obviously not the case since the key interpretation of a second calibration technique requires the measurement of the open alone and the subtraction of its

y-parameters from the DUT [WIJ87]. In this latter procedure known as the y-parameter subtraction technique, the parasitics in series with the bipolar transistor are assumed negligible.

For advanced BJTs, we propose that the most accurate interpretation of the s-parameter measurements is achieved by subtracting the y-parameters of the open as well as subtracting the z-parameters derived from measurement of the on-wafer shorts and thru from the DUT. When the physical origins of the y- and z-parameters are considered, it might be more desirable to use a three-step de-embedding procedure. This procedure includes first subtracting out the on-wafer open y-parameters shunting the input and output ports, next subtracting the z-parameters taken from the on-wafer thru and shorts, and finally subtracting the coupling capacitance between the input and output signal lines. This is a more general form of de-embedding and calibration because all parasitics associated with probe pads and interconnect-metal lines can be subtracted out of the measurement. In addition, for model development by the device engineer, a knowledge of the relative sizes and types (resistors and/or capacitors) of the BJT small-signal elements relative to the contact pad and interconnect parasitics can be helpful in estimating the experimental error and the sensitivity of the parameters of the DUT to the de-embedding procedure. We will present an equivalent circuit of the probe pad and interconnect

parasitics derived from s-parameter measurements using a special software package (MAESTRO) in conjunction with a small-signal model for the BJT. We find that the probe pad and interconnect parasitic elements at the BJT's output port are comparable to the equivalent BJT's small-signal elements and that blind use of the y-parameter subtraction technique can result in considerable experimental error.

2.2 Measurements

High frequency measurements (45 MHz - 26.5 GHz) were taken using an HP 8510 network analyzer with a HP4141B used for dc supply. Cascade Microtek ground-signal-ground (GSG) probes were mounted on an Electroglass probe station which was at dc ground and the entire apparatus was enclosed in a screen room. Two GSG probe heads were installed in the probe card. (The distance between heads is 250 μm and between tips is 200 μm.) Semirigid cables were used for the coaxial cable. Semirigid cables are mechanically suitable, since the probe heads are not significantly moved during operation. Most flexible cables are suitable if the cables are not moved or bumped during operation. An HP computer connected through an HPIB bus controls the equipments. The optimum operating parameters for measuring high-gain npn transistors in the network analyzer are shown in Table 2.1.

Table 2.1 The optimum operating parameters for HP8510 ANA.

PARAMETERS	VALUE
Source power level	10 dBm
Attenuation in port 1	-20 dBm
Attenuation in port 2	-20 dBm
Number of points	401
Source mode	step
Number of groups	1
Averaging number	128

The s-parameter measurements were calibrated up to the probe tips using an ISS (Cascade Microtek) calibration substrate using a full 2-port option in network analyzer. In full 2-port operation, six error coefficients are determined by measuring standards. Table 2.2 shows the error coefficients and their definitions. Reflection error coefficients, E_R, E_D and E_S, are determined by storing the reflection coefficients for reflection standards (OPEN, SHORT1 and SHORT2). Transmission error coefficients (E_T and E_C) are determined by measuring the THRU standard.

For evaluating these error coefficients exactly, it is important to define the calibration standard exactly to the network analyzer. The new definitions of the calibration standards for the probes used in the experiment are shown in Table 2.3. Resistors for the LOAD have been trimmed to 50Ω ± 0.1 %.

Table 2.2 The error definition for full 2-port calibration.

ERROR	DEFINITION
E_R	Error coefficient for cable and probe losses
E_D	Error coefficient for directivity errors
E_S	Error coefficient for source match error
E_T	Error coefficient for transmission response
E_L	Error coefficient for the opposite port match
E_X	Cross error coefficient

Table 2.3 The definition of the calibration standards of ISS.

STANDARDS	DEFAULTS	DEFINED VALUE
THRU	1 ps	2 ps
OPEN (Port 1)	-15 fF	-10 fF
OPEN (Port 2)	-15 fF	-15 fF
LOAD	50 Ω	50 Ω

After the calibration up to the probe tips, on-wafer dummies (open, short port 1, short port 2 and thru) are measured. For the purpose of knowing the parastic elements of the interconnects and pads, the equivalent circuit for the on-wafer open can be made by interpreting the measured data of on-wafer dummies (MAESTRO [VAI88]). The complete circuit for the on-wafer calibration standards (using the shorts and the thru to find the serial elements) will be discussed Section 2.4. Finally, the DUT (Device Under Test) is measured. The device reported on here had an emitter window opening 0.7 x 3.2 μm^2 and was biased from V_{BE} = 0.7 V to V_{BE} = 1.1 V and V_{BC} = -2 V but these results are not the exception.

Although the measurement resolution of the HP 8510 is 0.001 db, 0.01 degree and 0.01 ns [HP85], there can be larger experimental error because of the design of the experiment. For example, the on-wafer calibration patterns do not have the n/n^+ epitaxial layer which serves as the collector and buried layer for the DUT. Therefore, error is in de-embedding the DUT because the effect of the collector-to-substrate capacitance is not included in the measurement. In addition, there can be statistical fluctuations in the measurement, and process variation across the wafer can result in an error in de-embedding.

2.3 A General De-embedding Procedure

Layouts of on-wafer standards are shown in Fig. 2.1. It is known that the parasitics of the on-wafer open can be represented by y-parameter equivalent lumped elements in parallel to the bipolar transistor [WIJ87]. Because the relative size of the device is small, the series elements associated with the contact pads and interconnects cannot be neglected and the DUT measurement should be corrected for these in addition to shunt parasitics (y-parameter subtraction). Fig. 2.2 shows a more physical interpretation of the general lumped parasitics including the passive series elements of the interconnects and the passive shunt elements of the pads and interconnects. G_1, G_2 and G_3 represent the shunting

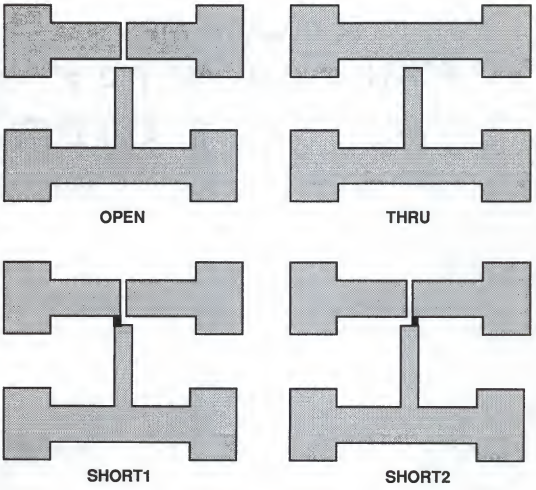


Figure 2.1 The layout of on-wafer standards; OPEN, SHORT 1, SHORT 2, THRU

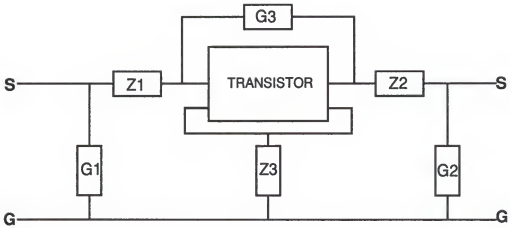


Figure 2.2 An equivalent circuit representation of the parasitic series impedance and shunt admittances of the contact pads and interconnects

parasitics of probe pads and interconnect lines. Since G_3 represents the coupling admittance between input and output port, this element is inside the series parasitics. Depending on the layout of on-wafer "open", the G_3 element can be put outside the series elements. For example, if the on-wafer "open" has probe pads but no interconnect line, the coupling admittance G_3 is for the pad-to-pad admittance. Therefore G_3 should be put outside the series elements. But in our case, the on-wafer 'open' has not only interconnect lines but also probe pads, G_3 represents the coupling admittance for the interconnect-to-interconnect line. From the y-equivalent circuit of the on-wafer 'open', the shunt parasitics become

$$G_1 = y_{11\text{open}} + y_{12\text{open}} \quad G_2 = y_{22\text{open}} + y_{12\text{open}} \quad G_3 = -y_{12\text{open}} \tag{2.2}$$

The first step in the three-step de-embedding procedure is to subtract out the shunting parasitics G_1 and G_2 from the experimental data of the DUT. The de-embedded DUT y-parameters are

$$\begin{aligned} y_{11} &= y_{11\text{m}} - G_1 \\ y_{22} &= y_{22\text{m}} - G_2 \end{aligned} \tag{2.3}$$

where the subscript m denotes the measured parameters.

The second step is to subtract out the series elements Z_1, Z_2 and Z_3 which are extracted as follows. In Fig. 2.3, the y_{12} (or y_{21}) of on-wafer 'thru' ($y_{12\text{thru}}$) is a equivalent

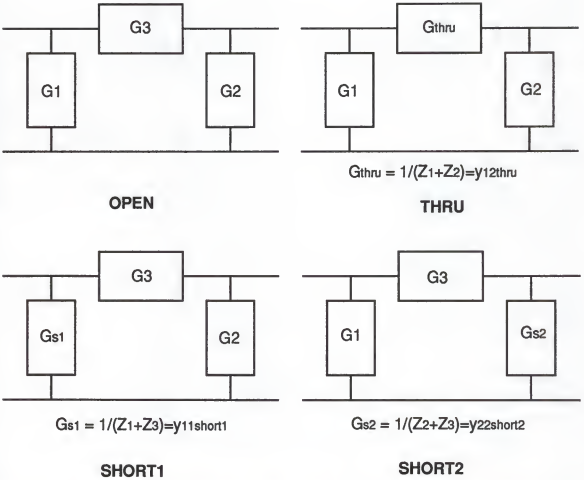


Figure 2.3 The y-parameter equivalent circuit representation of the OPEN, SHORTS and THRU

element to the top interconnect line (signal line). Therefore its inverse value can be considered as the sum of Z_1 and Z_2. In the same way, the inverse of the y_{11} of on-wafer 'short1' and the inverse of the y_{22} of on-wafer 'short2' is equivalent to input port (sum of Z_1 and Z_3) and output port (sum of Z_2 and Z_3), respectively. The resultant equations for Z_1, Z_2 and Z_3 are

$$Z_1 = \frac{1/y_{12\text{thru}} + 1/y_{11\text{short1}} - 1/y_{22\text{short2}}}{2}$$

$$Z_2 = \frac{1/y_{12\text{thru}} - 1/y_{11\text{short1}} + 1/y_{22\text{short2}}}{2} \qquad (2.4)$$

$$Z_3 = \frac{-1/y_{12\text{thru}} + 1/y_{11\text{short1}} + 1/y_{22\text{short2}}}{2}$$

Fig. 2.4 shows the extracted series reactance using this method. The optimized values for series inductance using curve fitting are 0.3, 0.25, and 0.15 nH for Z_1, Z_2 and Z_3, respectively. After extracting the series elements, the measured data can be corrected by z-parameter subtraction

$$\begin{aligned} Z_{11s} &= Z_{11} - Z_1 - Z_3 & Z_{12s} &= Z_{12} - Z_3 \\ Z_{21s} &= Z_{21} - Z_3 & Z_{22s} &= Z_{22} - Z_2 - Z_3 \end{aligned} \qquad (2.5)$$

where the terms on the right-side of the equations are the corrected z-parameters from step 1 and the series terms extracted using (2.4), and the terms on the left-hand side are the respective de-embedded terms. In the last step,

we correct the y-parameters of the de-embedded DUT for the $G_3 (y_{12open})$ term

$$\begin{aligned} y_{11} &= y_{11s} - G_3 & y_{21} &= y_{21s} + G_3 \\ y_{12} &= y_{12s} + G_3 & y_{22} &= y_{22s} - G_3 \end{aligned} \tag{2.6}$$

where the subscript s denotes the y-parameters obtained from the de-embedded z-parameters in (2.5) and the terms on the left-side of (2.6) are the de-embedded y-parameters.

2.4 Results and Discussion

In Fig. 2.5, the small-signal equivalent circuit of the BJT (in the dashed box) embedded in the optimized equivalent circuit for the open on-wafer calibration pattern is given. In Fig. 2.5, the small-signal equivalent circuit for the BJT represents the transistor operating at a bias condition (V_{BE} = 0.90 and V_{BC} = −2 V) equivalent to its peak frequency response f_T. It can be seen from the figure that the Miller capacitance (the 7.5 fF extrinsic base-collector capacitance in the figure) of the BJT dominates the input port of the DUT at the frequencies of interest. However, the parasitic capacitances of the probe pads and interconnects of the output port are larger than the BJT output (collector-substrate) capacitance. The measured output-port y-parameters of the on-wafer open are the same order of magnitude as the y-parameters of the DUT and much larger than the output-port

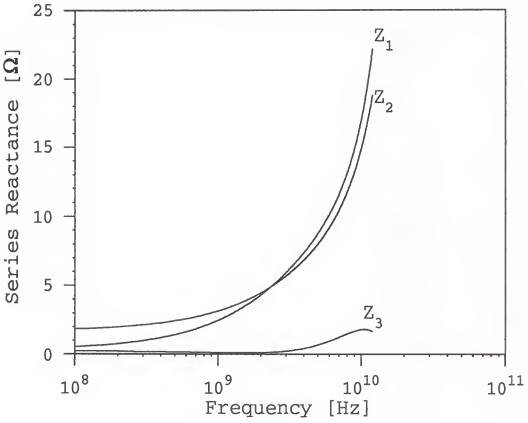


Figure 2.4 The extracted series reactance Z_1, Z_2 and Z_3 of the probe pads and interconnects.

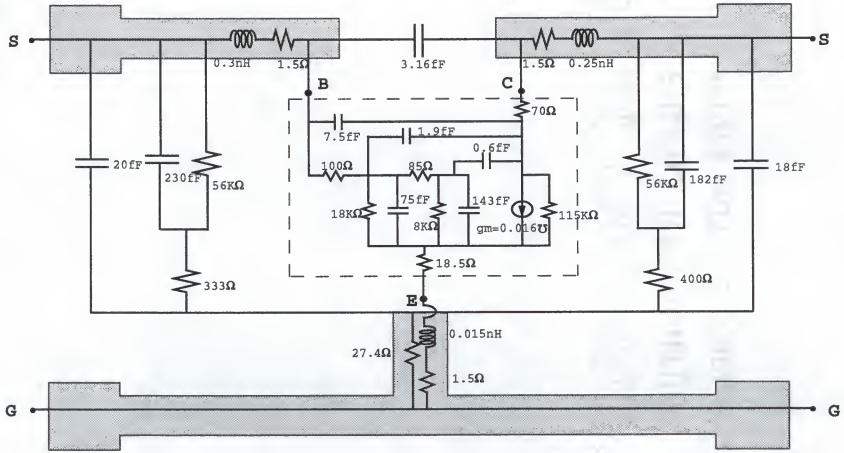


Fig.2.5 Small-signal equivalent circuit for DUT (in dashed box) and the contact pad and interconnect parasitics. The DUT is an npn transistor biased (Vbe=0.9 and Vbc=-2 V) at peak operating frequency.

y-parameters of the BJT. Therefore, errors in the measurement are magnified upon subtracting.

To figure out the consumed power in the environments of the device, the probe pad and interconnect of the input and output port are modeled as lossy transmission lines embedding the BJT. Fig. 2.6 shows that the s-parameters are measured at two planes by embedding the device in the transmission line structure. The s-parameter matrix, S', measured outside the transmission line is related to the s-parameter matrix of the device, S, by

$$S' = \Phi\, S\, \Phi$$
$$where \qquad \Phi = \begin{bmatrix} L_1 \epsilon^{-j\varphi_1} & 0 \\ 0 & L_2 \epsilon^{-j\varphi_2} \end{bmatrix} \tag{2.7}$$

where L_1 and L_2 represent the loss factor of the input and output, respectively. By carrying through the multiplication of the matrix,

$$S'_{11} = L_1^2\, S_{11}\, \epsilon^{-j2\varphi_1}$$
$$S'_{22} = L_2^2\, S_{22}\, \epsilon^{-j2\varphi_2} \tag{2.8}$$

L_1, L_2, φ_1 and φ_2 can be estimated from (2.8) in which S' represent the measured data and S represent the de-embedded data. The relative power loss due to the lossy interconnect and probe pad can be computed as

$$\begin{aligned} P_{loss}[dB] &= 10\, log\left(\frac{\Delta S_{11}\ \Delta S_{22}}{S_{11}\ S_{22}}\right) \\ &= 10\, log\left(\left|\frac{S_{11} - S'_{11}}{S_{11}}\right| * \left|\frac{S_{22} - S'_{22}}{S_{22}}\right|\right) \\ &= 10\left[log(1 - L_1^2) + log(1 - L_2^2)\right] \end{aligned} \tag{2.9}$$

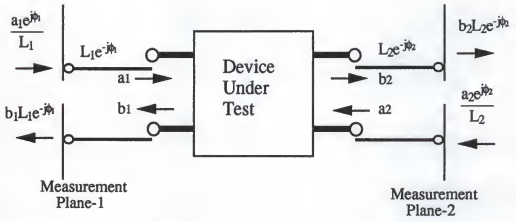


Figure 2.6 Two planes embedding the device in the lossy transmission line (L_1 and L_2 represent the lossy terms).

and the total phase shift due to the interconnect and probe pad ϕ_{total} becomes $\phi_1 + \phi_2$. The normalized power loss as a function of frequency for the probe pad and interconnect parasitics is given in Fig. 2.7. At high frequencies, the total power loss to the parasitics can be 60% of the power consumed in the device which is a significant fraction of the power consumption of the DUT. Because of the large loss in the probe pads and interconnects, we anticipate that there would be a significant difference between the embedded and de-embedded BJT data using our three-step de-embedding method or using y-parameter subtraction of the open on-wafer. This is confirmed in Fig. 2.8 which shows roughly a 67% discrepancy in the peak cut-off frequency f_T for the embedded and de-embedded responses and a $\sim$15% discrepancy in peak f_T between the two de-embedding (the three-step and the y-parameter subtraction) methods. This results show the series parasitics can not be neglected in high frequency operations.

In analog integrated circuit design, the measurements of the phase of the DUT's y-parameters are critical to accurate circuit modeling. In Fig. 2.9, the large discrepancy (10-30 degree differences) in the measured phases of y_{11}, y_{12} and y_{22} at the higher frequencies is demonstrated between the three-step method and the y-parameter subtraction method. The result is that the y-parameters interpreted using our

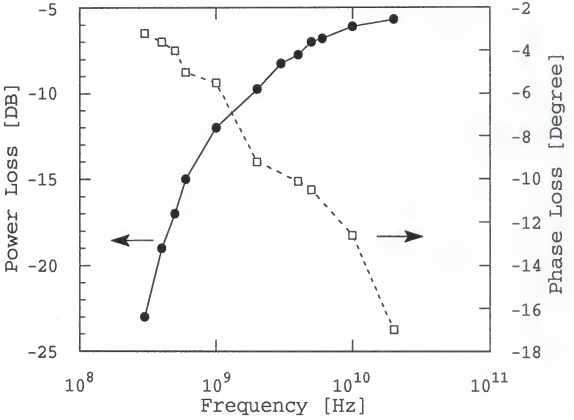


Figure 2.7 The magnitude and phase of the power lost to the contact pad and interconnect parastics of the input port as a function of frequency.

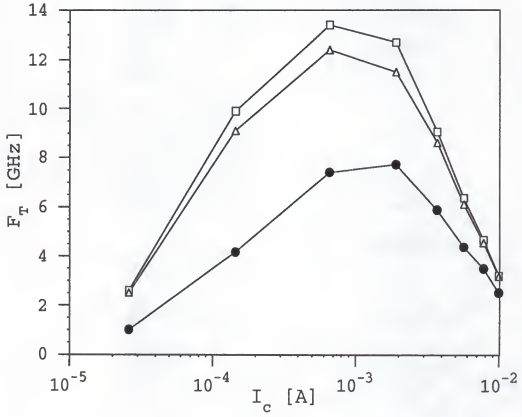


Figure 2.8 The unity gain frequency f_T as a function of collector current for the DUT. The raw data (-•-), the y-parameter de-embedded data (-△-) and the three-step de-embedding data (-0-) for the bias condition in Fig. 2.5.

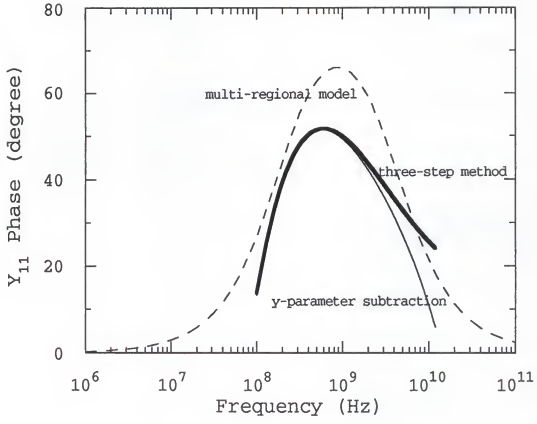


Figure 2.9 (a) A comparison of the phase taken using the y-parameter subtraction method and the three-step de-embedding method for y_{11}. The dashed line is the small-signal simulation from charge-based model [JO91].

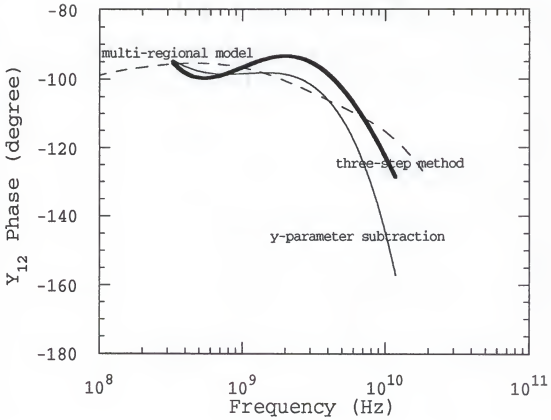


Figure 2.9 (b) A comparison of the phase taken using the y-parameter subtraction method and the three-step de-embedding method for y_{12}.

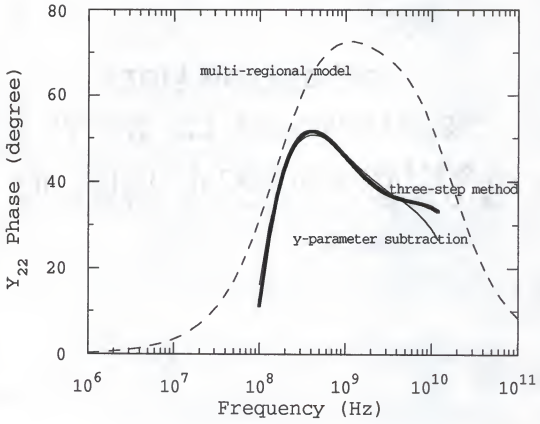


Figure 2.9 (c) A comparison of the phase taken using the y-parameter subtraction method and the three-step de-embedding method for y_{22}.

more general method are in better agreement with the small-signal model simulations of the BJT [JO91]. This further demonstrates the need for subtracting out the probe pad and interconnect parasitic series elements to accurately model the BJT. Compared to the y-parameter subtraction method, we expect our three-step de-embedding method to yield greater accuracy at higher frequencies and for narrower interconnect lines where the effect of the series parasitic elements increases concomitantly as the effect of the shunt elements decreases.

2.5 Conclusions

The accuracy of a three-step method for de-embedding s-parameter measurements of the DUT over the y-parameter subtraction of the open alone has been demonstrated. The three-step method includes the de-embedding of the parasitic shunt y-parameters of the on-wafer open calibration pattern as well as subtraction of the parasitic series z-parameters of the on-wafer shorts and thru from the DUT measurements. The additional subtraction of these parasitic series elements results in ~15% increase in peak f_T for de-embedded devices which have f_T > 10 GHz and ~10-30 degree difference in the phase of the de-embedded BJT y-parameters at the higher frequencies. The three-step method has been used in conjunction with MAESTRO to determine the magnitude and type of the interconnect and probe pad parasitics.

CHAPTER 3
A SIMPLE MODEL FOR DISTRIBUTED BASE IMPEDANCE WITH AC VERIFICATION USING S-PARAMETER MEASUREMENTS

3.1 Introduction

Since base resistance is a major element in the delay during high speed operation of bipolar junction transistors (BJTs) [TAN79], the exact extraction and modeling of the base resistance is important in small-signal BJT modeling. The base resistance depends on the effect of current crowding, where the current flows more toward the edge of the emitter because of a potential drop along the base region. There can be dc, ac and transient debiasing effects which result in emitter crowding. Only dc and ac crowding effects will be discussed herein. Ac crowding is strongly affected by the presence of dc crowding. In this case, the base-emitter diffusion capacitance at the edge of the emitter can be of the same order of magnitude as that at the center because of its proportionality to the collector current. Therefore, ac currents can experience a lower junction impedance at the edge of the emitter, which is termed ac crowding. For real-time ac circuit simulation, the base resistance has to be replaced by the base impedance which includes the effect of ac crowding.

Pritchard [PRI58] had analyzed the active base region as uniform transmission line when there is no significant

dc crowding. Ghosh [GHO65] had characterized two-dimensional base impedance as a parallel RC network including dc crowding. The capacitance in the base impedance emerges in the process of lumping the distributed elements into one element. Since modern BJTs have extremely narrow base widths and operate at high current densities, dc crowding and ac crowding effects are important and should be modeled properly.

The base resistance has been a difficult circuit element to measure due to its distributed nature and dependency on operating conditions. Several methods are available for measuring base resistance. There are four categories of methods. The first category is the use of noise measurements which measure base resistance using its effect on noise performance. The second is the pulse measurement which is appropriate for a switching application. The third obtains the base resistance from a plot of the dc current vs. emitter-base junction voltage. The final category uses the small-signal analysis. The two-port network method in this latter category is especially simple to apply and can be enhanced using the improved s-parameter interpretation of the previous chapter at the high frequencies.

In this chapter, the two-port network method is enhanced with a more accurate equivalent circuit. This more accurate equivalent circuit divides the BJT base-collector junction capacitance between both ends of the base resistance and then

the base resistance is updated with a complex base impedance. The base impedance is extracted from s-parameter measurements using this model. The s-parameter data is calibrated using the three-step de-embedding method presented in the previous chapter. This technique is preferred over the y-parameter subtraction of the 'open' calibration pattern [WIJ87] for small-signal model verification because (1) the magnitude of the interconnect and contact pad parasitics are determined and can be compared with the magnitudes of the device small-signal elements for the determination of experimental error and (2) the effects of the parastic inductive and resistive series elements are subtracted out of the data.

The active base region is divided mainly into the peripheral and intrinsic region. The peripheral transistor is more important and can not be neglected in modern BJT [REI84]. The intrinsic transistor can be divided into as many sections depending on the precision we want. We propose a simple model for the distributed quasi-3-dimensional base impedance including peripheral region and we show it to be self-consistent with the interpretation of the s-parameter measurements, the extraction of a lumped base impedance and a small-signal charge-based model proposed earlier [JO91].

The separation technique [REI84] between the peripheral and intrinsic transistor was proposed using the ratio of the emitter peripheral length to the emitter area. A new ac extraction method

from s-parameter measurement is developed in this chapter to check the validity of the separation.

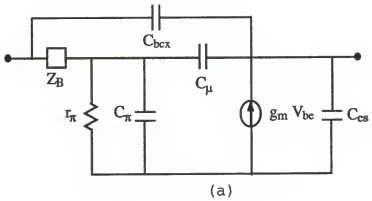
3.2 Extraction of AC Base Impedance

The modified two-port network method for more complete equivalent circuit is given in Fig. 3.1(a). This circuit has a base impedance Z_b instead of a base resistance R_b and includes the effect of a distributed base-collector junction capacitance, c_{bcx} (the extrinsic junction capacitance) and c_{μ} (the peripheral and intrinsic junction capacitance), which are normally lumped between external base and collector nodes in the conventional circuit model used for extraction of base impedance [GET79]. The resultant base resistance of the two-port network method without c_{μ} is

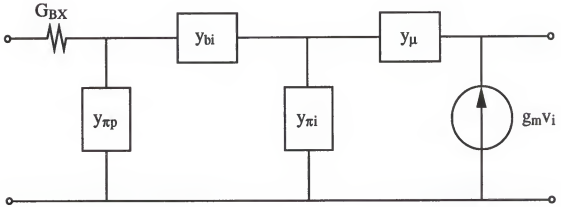
$$r_b = \frac{1}{g_m}\left\{ Real\left(\frac{y_{11}+y_{12}}{g_m+y_{12}-y_{21}}\right)\right\}^{-1} \tag{3.1}$$

The simulation shows that the base-collector junction capacitance c_{μ} has a major effect in extracting base impedance from measurements; at low bias conditions, the Miller capacitance $A_v c_{\mu}$ is comparable with c_{π} and can not be neglected. The y-parameters of Fig. 3.1(a) are

$$\begin{aligned} y_{11} &= jwc_{bcx} + \frac{1+jwc_t r_\pi}{r_\pi + Z_B + jwc_t r_\pi Z_B} \\ y_{21} &= (g_m - jwc_\mu)\frac{r_\pi}{r_\pi + Z_B + jwc_t r_\pi Z_B} - jwc_{bcx} \end{aligned} \tag{3.2}$$



(a)



(b)

Figure 3.1 (a) The lumped (peripheral and intrinsic transistor elements are lumped) equivalent circuit used for extracting the base impedance. (b) The distributed equivalent circuit used for extracting the base impedance.

$$y_{12} = -jw\left(c_{bcx} + \frac{c_\mu r_\pi}{r_\pi + Z_B + jwc_t r_\pi Z_B}\right)$$

$$y_{22} = (g_m - jwc_\mu)\frac{jwc_\mu r_\pi r_b}{r_\pi + Z_B + jwc_t r_\pi Z_B} + jw(c_\mu + c_{bcx} + c_{cs})$$

where $c_t = c_\pi + c_\mu$, g_m and c_{cs} are taken from multi-regional model. The resulting expression used for the extraction of a lumped base impedance is

$$Z_B = \frac{1}{G_\pi + jw(C_\pi + C_\mu)}\frac{g_m - y_{21} + y_{12}}{y_{21} - y_{12}} \tag{3.4}$$

where

$$G_\pi = g_m\, Real\left[\frac{y_{11} + y_{12}}{y_{21} - y_{12}}\right] \tag{3.5}$$

$$C_\pi = \frac{g_m}{w}\, Imag\left[\frac{y_{11} + y_{12}}{y_{21} - y_{12}}\right] \tag{3.6}$$

$$C_\mu = \frac{1}{jw}\frac{g_m(G_\pi + jwC_\pi)(y_{22} + y_{12} - jwC_{cs}) + jwg_mC_{cs}}{(g_m + G_\pi + jwC\pi)(g_m - y_{21} + y12) - g_m(y_{22} + y_{12})} \tag{3.7}$$

where c_μ is a complex quantity.

Equation (3.3) is consistent with the conventional method when c_μ is neglected. If we neglect c_μ from (3.3),

$$Z_B = \frac{1}{G_\pi + jwc_\pi}\frac{g_m - y_{21} + y_{12}}{y_{21} - y_{12}}$$

$$= \frac{\frac{g_m - y_{21} + y_{12}}{y_{21} - y_{12}}}{g_m Real\left[\frac{y_{11} + y_{12}}{y_{21} - y_{12}}\right] + jg_m Imag\left[\frac{y_{11} + y_{12}}{y_{21} - y_{12}}\right]} \tag{3.8}$$

$$= \frac{1}{g_m}\frac{g_m - y_{21} + y_{12}}{y_{11} + y_{12}}$$

of which the real part is same as in Eq. (3.1). The base impedance, Z_B, is obtained from four y-parameters converted from s-parameter measurements for the device in the common-emitter configuration.

In Fig. 3.2, the experimental data as a function of V_{BE} is shown for frequencies above 0.1 f_T where f_T for these advanced BJTs (1.5 x 4 μm) is above 10 GHz. The magnitudes of base impedance at 0.1 f_T are consistent with the dc model [JO90]. The data show that as frequency increases, the magnitude of Z_B is reduced and saturates above about 10 GHz. Since the conductivity modulation of the peripheral base region is still important, the saturated values are dependent on bias condition at these frequencies.

Fig. 3.3 shows the difference of extracted base impedance using Eq. (3.1) and Eq. (3.3) using the same s-parameter data. The data show that at low biases there is a big difference between the extracted base impedances. It is clear that $c_{//}$ cannot be neglected at low bias.

To extract the base impedance from s-parameter measurement, it is critical to de-embed the probe pad and interconnect parastics to obtain the exact 2-port parameter of the transistor. The contact pad and interconnect parastics are shown in Fig. 2.5. Although the series inductances are less than a nanohenry, if not properly subtracted out of the data, they can have a large effect on the phase of the extracted base impedance. The difference in phase between the two techniques is given in Fig. 3.4. Physically, at very high frequencies, the phase of Z_B approaches

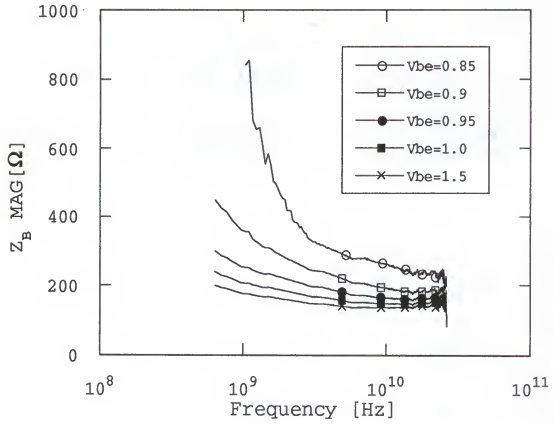


Figure 3.2 The extracted base impedance value for different bias condition. The device size is 1.5x4 μm and V_{BC} = −2 V.

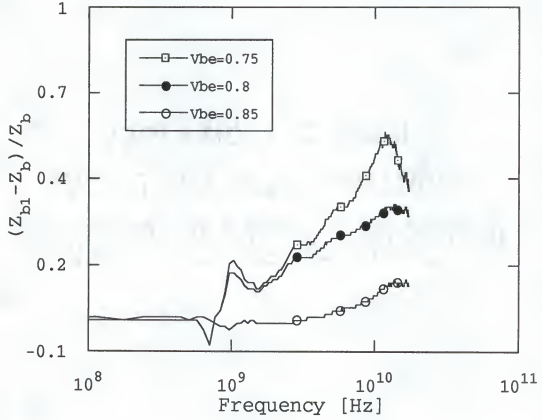


Figure 3.3 A comparison of two different extraction methods of base impedance at different bias condition. Z_b is the extracted base impedance using our method. Z_{b1} is that of conventional method.

0 degree because the shunt capacitance is practically shorted and only the extrinsic resistances (including peripheral resistance) are in the input port. If the inductive parasitics are not subtracted out, the phase of Z_B is well beyond the 0 degree at high frequencies. It is approximately 30° at the higher measurement frequencies. This difference can be significant in interpreting the transistor model.

3.3 Simulation

3.3.1 Simulation with Existing Model

The modeling of base resistance, which is associated with emitter crowding, is essential for large-signal and small-signal BJT modeling. The large-signal model for base resistance has been developed for low through high current BJT operation [J090]. High current effects, which are base push-out into the collector region and high level injection, are included in this model. Also this base resistance model includes the conductivity modulation of the base region and dc emitter current crowding.

In the hybrid-π model, the base resistance is treated as a single lumped resistance r_b, but, in high frequency operation, the bipolar transistor can be represented by more and more circuit elements distributed as a function of distance from base contact. The large-signal model for base resistance is not sufficient for modeling these distributed elements at high frequencies.

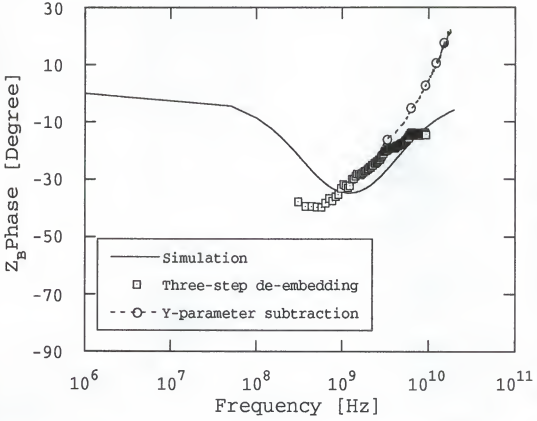


Figure 3.4 A comparison of two calibration technique: (1) y-parameter subtraction and (2) three-step de-embedding method.

Therefore, a base impedance model for small-signal which is consistent with the large-signal base resistance at dc or low frequencies is needed.

A schematic of the circuit model for distributed base region is given in Fig. 3.5(a). The small-signal elements of this circuit are derived from a novel multi-regional charge-based bipolar model reported on earlier [J091]. This multi-regional circuit model has elements for extrinsic base-collector diode, the peripheral and intrinsic transistor. The peripheral transistor charges and currents are proportional to the equivalent intrinsic transistor charges and currents. The charge-based approach is much more physical than the conventional charge-control (Gummel-Poon) approach and accurately accounts for high injection in the base and collector regions. The intrinsic transistor model [JE089] is derived from a one-dimensional regional analysis of the ambipolar carrier transport and the key model parameters for both this model and the multi-regional model are taken primarily from layout and processing information. The emitter, base and collector recombination lifetimes are the only explicit time constants, i.e., the other delays are implicitly taken into account in the charge dynamics.

When the transistor is divided into peripheral and intrinsic transistor, the base region is implicitly modeled quasi-three-dimensionally since the peripheral region adds one more dimension. In the quasi-three-dimensional approach, since

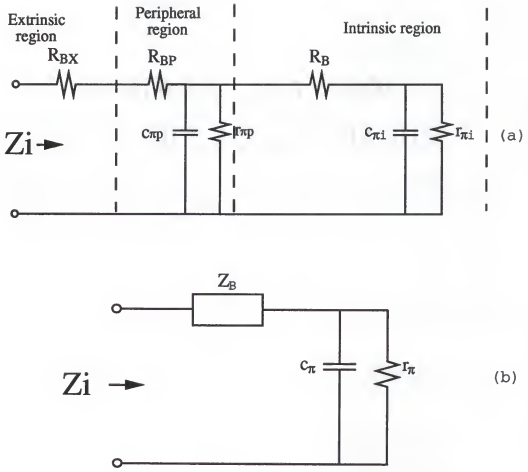


Figure 3.5 (a) The distributed model for the base region. R_{bx} is the extrinsic base resistance; p and i represents the peripheral elements and intrinsic elements respectively. (b) The lumped model for the base-emitter junction.

the collector current of peripheral transistor is 20 ~ 30 % of that of intrinsic transistor, the diffusion capacitance of peripheral transistor is sometimes comparable to that of intrinsic transistor. Because of the peripheral diffusion capacitance and the sheet resistance between peripheral and intrinsic region, the ac current crowding effect is different from that of the two-dimensional approach.

R_{bp}, the peripheral resistance, is neglected in the large-signal model. But as shown in Fig. 3.2, the saturated values of the base impedance data at high frequencies are the function of bias condition. Therefore, the peripheral resistance cannot be neglected at high frequencies and can be roughly modeled by $F^*(R_{BI}I_{cp})/I_{cI}$ where I_{cI} is the current of intrinsic transistor and F is a constant depending on the doping concentration of peripheral region to the intrinsic region.

In the lumped model in Fig. 3.5(b), Z_b represents the base impedance for the extrinsic (R_{bx}), peripheral and intrinsic base region. Since both circuits in Fig. 3.5 are equivalent, the short-circuit input impedance should be same. The input impedance of Fig. 3.5(a) is

$$Z_{in_{ts}} = R_{BX} + R_{BP} + \frac{R_{BI}^{-1} + Y_{\pi i}}{Y_{\pi i}(R_{BI}^{-1} + Y_{\pi p}) + Y_{\pi p}R_{BI}^{-1}} \tag{3.9}$$

where

$$\begin{aligned} Y_{\pi i} &= r_{\pi i}^{-1} + jwc_{\pi i} \\ Y_{\pi p} &= r_{\pi p}^{-1} + jwc_{\pi p} \end{aligned} \tag{3.10}$$

Therefore, Z_b can be calculated by subtracting the impedance of r_π and C_π in Fig. 3.5(b) from the short-circuit input impedance of distributed circuit in Fig. 3.5(a). Therefore,

$$Z_B = Z_{idis} - \frac{r_\pi}{1 + jwr_\pi c_\pi} \tag{3.11}$$

where $r_\pi = r_{\pi p} \,||\, r_{\pi i}$, $C_\pi = C_{\pi p} + C_{\pi i}$.

Fig. 3.6 shows the simulation and experimental data at V_{EB} = 0.9 V. Simulation shows some discrepancy with the measured data. There can be two possible explanations for this discrepancy. The one is the separation technique used in this model for peripheral and intrinsic capacitances because the value of peripheral capacitance is very important in the above simulation. The other is the base resistance value between the peripheral and intrinsic transistor. Since the base resistance model [JO90] can be applicable to the lumped model, the resistance between peripheral and intrinsic region can be evaluated according to the base resistance model.

3.3.2 Modification of the existing model

The intrinsic base resistance [JO90], R_{BI}, between the peripheral transistor and the intrinsic transistor can be the base resistance seen outside the peripheral transistor. In that case, we can figure out the resistance between the peripheral and intrinsic transistor by equating the short-circuit input

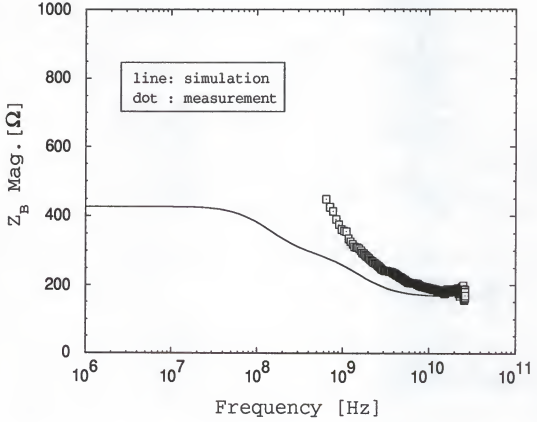


Figure 3.6 The comparison of simulation and experimental data at V_{EB}=0.9 V.

impedance of the distributed circuit at dc to the R_{BI} plus r_π where r_π is $r_{\pi p}$ || $r_{\pi i}$.

$$R = \frac{(R_{BI} + r_\pi)(r_{\pi i} + r_{\pi p}) - r_{\pi i} r_{\pi p}}{r_{\pi p} - R_{BI} - r_\pi} \tag{3.12}$$

These values of R are higher than the values of R_{BI} and R replaces the R_{BI} in the equivalent circuit of Fig. 3.5 (a).

In Fig. 3.7, the simulations using this method are shown to be in good agreement with the experimental data.

Based on the above discussion, an analytical form for the base impedance Z_B can be derived. For high frequencies which satisfy the following conditions, $\left|\frac{1}{jwc_{\pi i}}\right| < r_{\pi i}$ and $\left|\frac{1}{jwc_{\pi p}}\right| < r_{\pi p}$, the $r_{\pi i}$ and $r_{\pi p}$ can be neglected. Therefore, the input impedance of the distributed model of Fig.3.1(a) is

$$Z_i = R_{bp} + R_{bx} + \frac{1 + jwc_{\pi i}R}{jw(c_{\pi i} + c_{\pi p}) - Rw^2 c_{\pi i} c_{\pi p}} \tag{3.13}$$

Then the base impedance can be calculated by subtracting the c_π of Fig. 3.5(b) from Z_i, where r_π of Fig.3.5(b) is neglected since $\left|\frac{1}{jwc_\pi}\right| = \left|\frac{1}{jw(c_{\pi i}+c_{\pi p})}\right| < r_{\pi i} < r_\pi$:

$$Z_B = R_{bx} + R_{bp} + \frac{R\left(1 - \frac{c_{\pi p}}{c_\pi}\right)/\left(1 + \frac{c_{\pi p}}{c_{\pi i}}\right)}{\left[1 + \left(\frac{w}{w_{ref}}\right)^2\right]^{1/2}} \tag{3.14}$$

where

$$w_{ref} = \frac{1 + \frac{c_{\pi p}}{c_{\pi i}}}{Rc_{\pi p}} \tag{3.15}$$

Fig. 3.8 compares this analytical equation with simulated data. The data show a good agreement within a 5% error range.

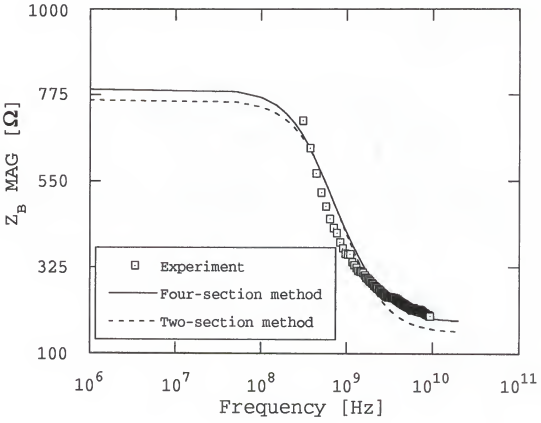


Figure 3.7 (a) Comparison of the experimental data and simulation data (magnitude). The two section method is for a transistor divided into one peripheral and one intrinsic region. The four section method is for a transistor divided into one-peripheral and three intrinsic regions.

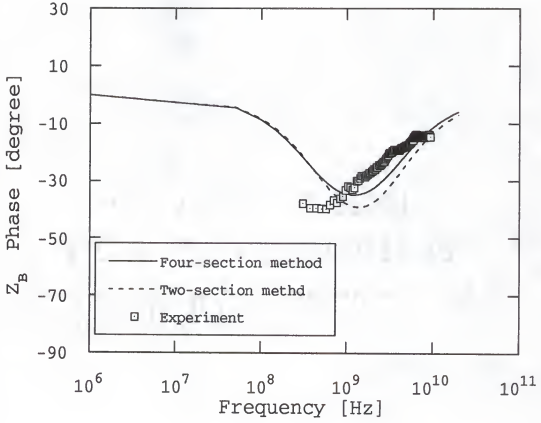


Figure 3.7 (b) Comparison of the experimental data and simulation data (phase).

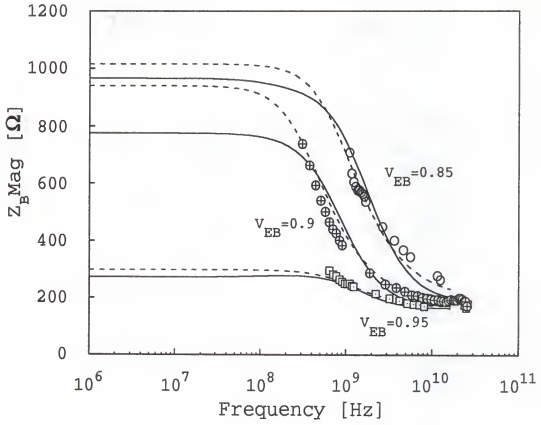


Figure 3.8 Comparison of the experimental data, simulation data and simplified model data at different bias conditions.

We can anticipate a better simulation by subdividing the intrinsic region further. At the high frequencies, input resistances, $r_{\pi i}$ and $r_{\pi p}$, can be neglected. Each section in the intrinsic transistor is characterized by its proportional share of collector current as calculated from the charge-based model. Each section is separated from adjacent section by a physical base resistance. This resistance is not the same for each section because of the differences in conductivity modulation and should be modeled properly. Since the base resistance is roughly proportional to the inverse of collector current, the physical resistance of each section can be set by some proportion of that of the most outside section (the edge section) of the intrinsic transistor depending on the collector current share. Therefore, if the physical resistance of the base is represented by R, the resistance of the first section, the second section, etc. can be represented by

$$R_1 = \frac{\frac{1}{f_1}}{\frac{1}{f_1}+\frac{1}{f_2}+\frac{1}{f_3}+\cdots} R$$
$$R_2 = \frac{\frac{1}{f_2}}{\frac{1}{f_1}+\frac{1}{f_2}+\frac{1}{f_3}+\cdots} R \qquad (3.16)$$
$$\cdots$$

where the values f_1, f_2, etc. are the proportion of current of each respective section compared to the total collector current.

Figure 3.7 shows the four-section simulation with the measured data. Some refinement is shown over the two-section method but less than expected.

In our quasi-three-dimensional approach, the relative magnitudes of peripheral diffusion-capacitance impedance and the physical base impedance results in ac current crowding at the peripheral region. Therefore, the effect on ac crowding of the intrinsic region is not as important for these devices. This effect can be shown by comparing the simulations using the two-section method (the peripheral transistor plus a intrinsic transistor) and the four-section method (the peripheral transistor plus three intrinsic transistor sections). The Z_b from the four-section method is almost the same as that from two-section method, especially in magnitude. Since the phase is more sensitive to the magnitude and type as well as the distribution of the intrinsic transistor elements, the phase of Z_b is different for these two methods. Any error between measurement and simulation of the phase of Z_b is attributed to the inaccuracies in the multi-regional BJT model parameters and not to the experimental technique described here.

3.3.3 Extraction from A Distributed Equivalent Circuit

To check the validity of proper separation between the peripheral transistor and intrinsic transistor, all the circuit elements are extracted from s-parameter measurement.

Partitioning the transistor into the intrinsic and extrinsic regions is a more physical method to model the small-signal of the

modern bipolar transistor than a lumped model. This partitioning involves more parameters and elements, i.e., intrinsic base resistance, the separation of the junction capacitance, the emitter time constants and the electron or hole diffusivity of the intrinsic and peripheral transistor regions needed to evaluate diffusion capacitance. Rein [REI84] proposed the experimental method to separate the collector current and base current between peripheral and intrinsic transistor. Since the diffusion capacitances depend on the collector current of each region and the empirical emitter time constants in the charge-based model [JO91], it is hard to verify the capacitance value.

We develop an extraction method of the device elements from the s-parameter measurement. The device elements include intrinsic base resistance and base capacitance (R_{bi} and C_{bi}) that comprise the base impedance, the input conductance and capacitances of the peripheral and intrinsic transistor (R_{pip}, C_{pip}, R_{pi} and C_{pi}). The equivalent circuit of the bipolar transistor is shown in Fig. 3.1(b). The boxes in this circuit represents admittances (which are assumed to be a parallel RC network). The y-parameters of this circuit are

$$\begin{aligned} y_{11} &= y_{\pi p} + \frac{y_{bi}(y_{\pi i} + y_{\mu})}{y_{bi} + y_{\pi i} + y_{\mu}} \\ y_{21} &= -\frac{(g_m + y_{\mu})y_{bi}}{y_{bi} + y_{\pi i} + y_{\mu}} \\ y_{12} &= -\frac{y_{bi}y_{\mu}}{y_{bi} + y_{\pi i} + y_{\mu}} \\ y_{22} &= \frac{-g_m y_{\mu} + y_{\mu}y_{bi} + y_{\mu}y_{\pi i}}{y_{bi} + y_{\pi i} + y_{\mu}} \end{aligned} \tag{3.17}$$

where

$$y_{\pi p} = r_{\pi p}^{-1} + jwc_{\pi p} \qquad y_{\pi i} = r_{\pi i}^{-1} + jwc_{\pi i}$$
$$y_{\mu} = r_{\mu}^{-1} + jwc_{\mu} \qquad y_{bi} = r_{bi}^{-1} + jwc_{bi} \tag{3.18}$$

The extracted elements from these equations are

$$\begin{aligned} g_m &= y_{\mu}\frac{y_{21} - y_{12}}{y_{12}} \\ y_{bi} &= -\frac{(y_{21} + y_{22})(g_m + y_{\mu})}{g_m + y_{\mu}\frac{y_{22}+y_{12}}{y_{12}} - \frac{y_{22}(y_{21}+y_{22})}{y_{12}}} \\ y_{\pi i} &= g_m - y_{bi}\frac{y_{22} + y_{12}}{y_{12}} \\ y_{\pi p} &= y_{11} - \frac{y_{bi}(y_{\pi i} + y_{\mu})}{y_{bi} + y_{\pi i} + y_{\mu}} \end{aligned} \tag{3.19}$$

when y_{μ} is given.

To make calculation simple, these y-parameters are evaluated without including the extrinsic base resistance G_{bx}. The y-parameters should be changed to include G_{bx}

$$y_{11} = \frac{y_{11m}G_{bx}}{G_{bx} - y_{11m}} \qquad y_{21} = \frac{y_{21m}G_{bx}}{G_{bx} - y_{11m}}$$
$$y_{12} = \frac{y_{12m}G_{bx}}{G_{bx} - y_{11m}} \qquad y_{22} = \frac{y_{22m} + y_{12m}y_{21m}}{G_{bx} - y_{11m}} \tag{3.20}$$

where the subscript m denotes measured data. Therefore, the device elements are extracted using (3.18) and the y-parameters of (3.19).

Each admittance block (Y_{bi}, $y_{\pi i}$ and $y_{\pi p}$) can be decomposed into a parallel RC network. Therefore all elements can be extracted from measurement.

Fig. 3.9 and Fig. 3.10 show the extracted elements as functions of frequency for the device size 1.5x4 μm^2 and and 1.5x8 μm^2 at

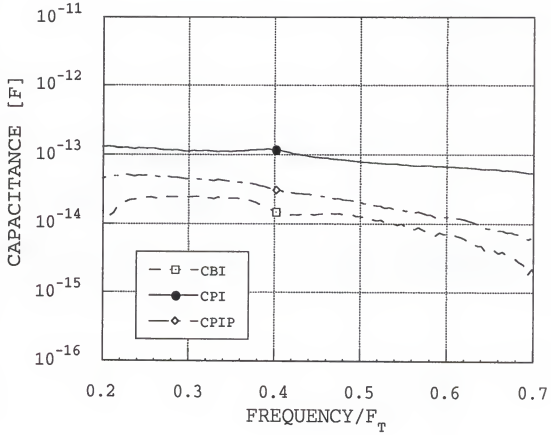


Figure 3.9 The extracted capacitances as a function of frequency (1.5x4 μm^2).

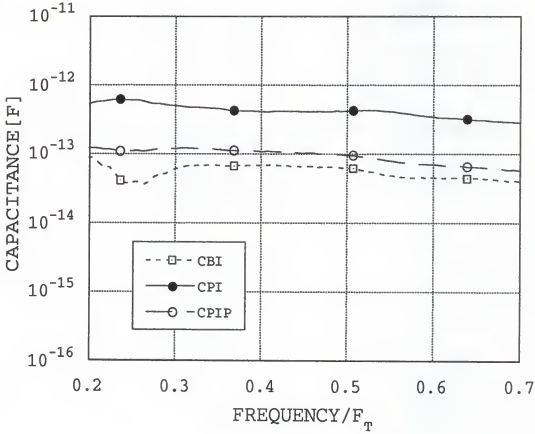


Figure 3.10 The extracted capacitances as a function of frequency (1.5x8 μm^2).

V_{EB}=0.85V and V_{BC}=-2 V. The capacitance values are reasonably constant over $0.1f_T$ ~ $0.9f_T$ and are of the same order as simulated data [JO91]. But the resistance values except R_{bi} are changing over a wide range, which implies the capacitance is dominant at the high frequency region. Table 3.1 show the extracted data and simulated data. The capacitance values in the intrinsic region are comparable but the peripheral capacitance values are different. R_b and R_{bp} are the intrinsic and peripheral base resistances of modified model.

Fig. 3.11 shows the capacitance values and base resistance as a function of bias. The value of base resistance is the same order as in published data [JO90]. But at high frequency, the parallel capacitance C_{bi} is dominant over the base resistance. Therefore, the overall base impedance is reduced as a function of frequency. This capacitance accounts in part for ac crowding [GH065] in the transistor.

Fig. 3.12 shows the input impedance of our modified model and extracted equivalent circuit using (3.18). This agreement shows the base impedance can be modeled either by modifying the intrinsic base resistance without changing the other device elements (Topic 3.3.2) or by modifying the peripheral capacitance value with base impedance (RC parallel network). Also, this extraction method can be a verification tool in partitioning of the transistor into intrinsic and extrinsic transistor.

Table 3.1 (a) Extracted value of device elements (1.5x4 μm^2)

V_{EB}	$C_{\pi i}$	$C_{\pi p}$	C_{bi}	r_{bi}	C_{μ}
0.85	2.7E-13	7.4E-14	4.9E-14	423.6	5E-14
0.9	6.4E-13	9.7E-14	7.9E-14	316	6E-14
0.95	2.0E-12	6.0E-13	1.1E-12	53	8E-14
1.0	3.7E-12	1.6E-12	3.5E-12	35	8E-14

Table 3.1 (b) Simulated values of device elements (1.5x4 μm^2) without c_{bi}

V_{EB}	R_b	R_{bp}	r_{bi}	$C_{\pi i}$	$C_{\pi p}$
0.85	1798.91	110.65	775	2.35E-13	1.12E-13
0.9	1639.41	90.1271	604.6	6.2E-13	2.85E-13
0.95	260.21	82.41	110.82	2.06E-12	8.3E-13
1.0	100.97	28.1	44.3	3.95E-12	1.6E-12

Table 3.1 (c) Extracted values of device elements (1.5x8 μm^2)

V_{EB}	$C_{\pi i}$	$C_{\pi p}$	C_{bi}	r_{bi}	C_{μ}
0.8	1.5E-13	5.9E-14	2.46E-14	334	5E-14
0.85	4.98E-13	1.2E-13	6.48E-14	225	5E-14
0.9	7.6E-13	1.7E-13	1.07E-13	155	6E-14
0.95	5.6E-12	1.5E-12	2.3E-12	36	1.E-13

3.4 Conclusions

The quasi-three-dimensional base impedance is characterized by sectioning the base region. Since the collector current of the peripheral transistor is 20 ~ 30 % that of intrinsic transistor, the diffusion capacitance of the peripheral transistor is sometimes comparable to the diffusion capacitance of the edge

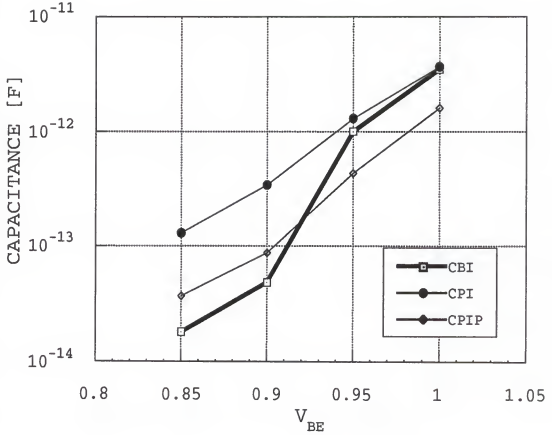


Figure 3.11 The extracted capacitances as a function of bias (1.5x4 μm^2).

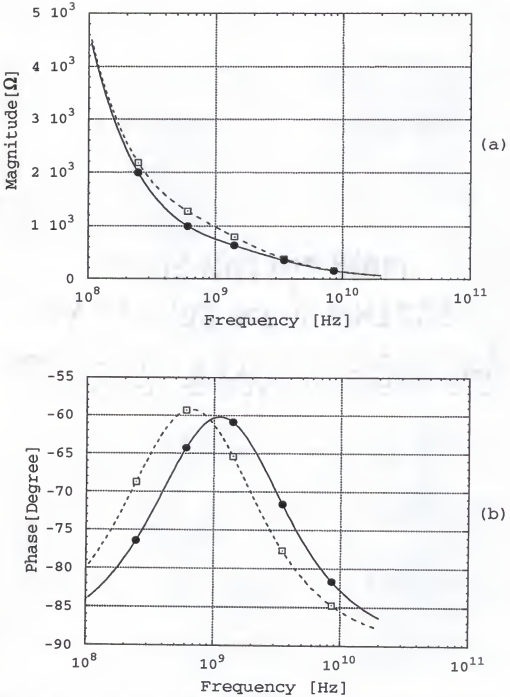


Figure 3.12 The comparison of the (a) magnitude and (b) phase of the input impedance of our modified model and equivalent circuit using elements extracted from (3.19).

region of the emitter. Therefore, it can not be neglected. From comparing the base impedance simulated with varying numbers of transistor sections, we can see the peripheral region is important in high frequency operation.

The advantages of the approach represented herein are (1) since this model for base impedance includes the peripheral and intrinsic transistors, it is more complete; (2) it is more physical since it is based on the charge-based BJT model; and (3) it is simple and does not require exorbitant computational time.

Therefore, we conclude that (1) the two-section method is sufficient for modeling advanced BJT and (2) the peripheral transistor is important at higher frequencies.

CHAPTER 4
A CHARGE-BASED MODEL FOR LATERAL PNP TRANSISTOR

4.1 Introduction

In many circuit applications, the lateral pnp transistor is widely used as complementary transistor because it has fabrication steps that are compatible with those of the vertical npn. Since integrated circuits are now more and more complex, an accurate model for lateral pnp is needed for computer-aided circuit design.

Lindmayer and Schneider [LIN67] separated the emitter current into two independent components: a lateral and a vertical component. They only accounted for the lateral component of collector current, but in reality a more vertical component is also present along the curved trajectory underlying the emitter and collector junctions and this results in a two-dimensional collector current. Chou [CHO71] introduced the experimental 2-D geometrical factor F_{GC} by varying epitaxial thickness W_{epi} and minimum base width W_{bo} ratio respect to junction depth x_j. Seo and Kim [SEO80] developed an analytical model for the lateral collector current. One can easily see from the 2-D simulation, i.e., PISCES, that the hole current flow can be roughly divided into two components: a purely lateral flow I_{CL} in the emitter sidewall region and a flow along the curved trajectory I_{CV} under

the emitter as shown in Fig. 4.1. Fig. 4.1 shows a structure for the lateral pnp to be used in this chapter.

This chapter presents analytical geometrical factors for the lateral current F_{GCL} and the vertical current F_{GCV}. These geometrical factors include the two-dimensional effects in the lateral pnp. Therefore, the total collector current is calculated by multiplying one-dimensional current by geometrical factors.

A purely lateral current which flows parallel to the surface is modeled as a function of the varying base width due to lateral diffusion in the emitter and collector region. The curved trajectory under the emitter is modeled by concentric curvature of which the center point is located at $(W_{bo}/m)+x_j$ above the midpoint of the distance between the bottom junction of emitter and collector. Major parameters for layout geometry are minimum base width W_{bo}, epitaxial thickness W_{epi} and junction depth x_j.

These geometrical factors are also functions of bias condition since W_{bo} and W_{epi} vary according to the bias of each junction. In turn, the bias of each juction is affected by the collector current and base current, i.e., voltage drop across R_e and R_b. Since they are all related to each other, an iterative procedure is necessary to find the internal bias. Therefore, it is essential to have a analytical geometrical factor in our semi-numerical approach.

The vertical collector and base current dominate at the higher current levels when the voltage drop across the lateral emitter resistance, R_{elat}, causes a reduction in the sidewall junction

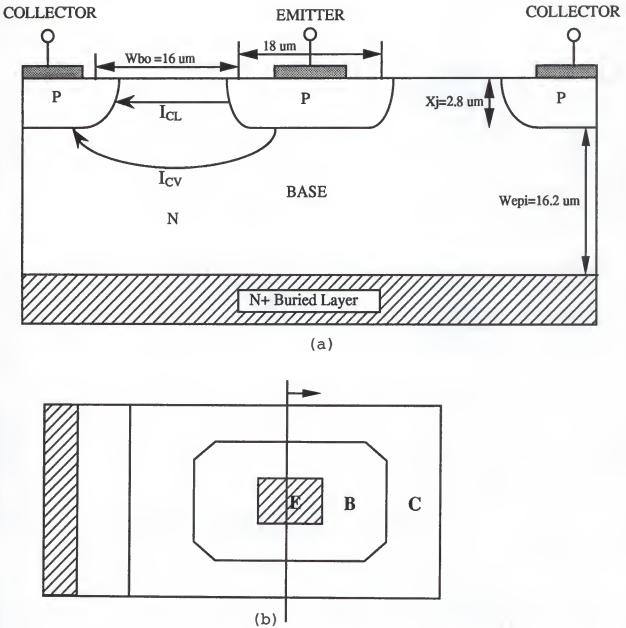


Figure 4.1 (a) Cross-section of lateral pnp transistor. Flow lines for the vertical and lateral components of collector current are shown on the figure. (b) Top view of lateral pnp transistor. The collector completely surrounds the emitter region to improve current gain.

bias and, hence, the lateral collector current. This phenomenon explains current gain falloff at high current levels in addition to the high level injection in one-dimensional I_{co}.

In Section 4.2, the geometrical factors F_{GCL} and F_{GCV} are derived analytically and compared to that of Chou [CHO71]. These models for geometrical factors can be applied to general geometry lateral transistors, for example, lateral npn transistor in CMOS well. Section 4.3 and 4.4 show in detail how the collector and base current are calculated. The current of parasitic substrate p-n-n^+—p transistor is derived in Section 4.5. The results are shown in Section 4.6. Transient modeling and small-signal modeling is shown in Sections 4.7 and 4.8, respectively.

4.2 Geometric Factors

4.2.1 Lateral Geometric Factor

One-dimensional current I_{co} is given by [GRO67]

$$I_{co} = qp'_{ne}\frac{D_p}{W_{bo}}l_e x_j \tag{4.1}$$

In the above equation, p'_{ne} is the injected hole concentration at the emitter-base junction and $l_e x_j$ is the area of the emitter junction sidewall.

The geometry of the emitter and collector sidewall is shown in Fig. 4.2. The curved junctions on both sides are considered to be cylindrical with radius of curvature x_j. In Fig. 4.2, the base

width W_b is a function of x

$$W_b(x) = W_{bo} + 2x_j(1 - cos\theta)$$
$$where \quad \theta = sin^{-1}\left(\frac{x}{x_j}\right) \tag{4.2}$$

The lateral collector current can be formulated

$$I_{cl} = l_e \int_0^{x_j} \vec{J}_c \cdot \vec{dy}\, dx \tag{4.3}$$

Since the lateral current is assumed purely parallel to the surface, $J_c = |J_c|\,\vec{dy}$. Therefore, the lateral collector current becomes

$$\begin{aligned} I_{cl} &= l_e \int_0^{x_j} |J_c|\, dx \\ &= qp'_{no} D_p l_e \int_0^{x_j} \frac{dx}{W_b(x)} \end{aligned} \tag{4.4}$$

The integration becomes

$$\begin{aligned} \int_0^{x_j} \frac{dx}{W_b(x)} &= x_j \int_0^{\frac{\pi}{2}} \frac{cos\,\theta\ d\theta}{(W_{b0} + 2x_j) - 2x_j cos\,\theta} \\ &= -\frac{1}{2}\left[\frac{\pi}{2} - \left(1 + \frac{W_{b0}}{2x_j}\right) \frac{2\,tan^{-1}\sqrt{\frac{2 + \frac{W_{b0}}{2x_j}}{\frac{W_{b0}}{2x_j}}}}{\sqrt{\left(1 + \frac{W_{b0}}{2x_j}\right)^2 - 1}}\right] \end{aligned} \tag{4.5}$$

The lateral geometric factor F_{GCL} turns out to be

$$\begin{aligned} F_{GCL} &= \frac{I_c}{I_{co}} = \frac{a}{2}\left[\frac{a+2}{\sqrt{\left(1 + \frac{a}{2}\right)^2 - 1}}\, tan^{-1}\sqrt{1 + \frac{4}{a}} - \frac{\pi}{2}\right] \\ where \quad a &= \frac{W_{bo}}{x_j} \end{aligned} \tag{4.6}$$

We can see the lateral geometrical factor only depends on the ratio of minimum base width to junction depth.

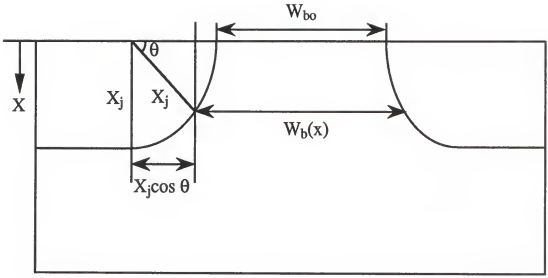


Figure 4.2 The geometry of emitter and collector sidewall of lateral pnp transistor. The base width W_b is a function of x. W_{bo} is a minimum base width and x_j is a junction depth.

4.2.2 Vertical Geometric Factor

The vertical collector current path can be modeled by concentric curves with the radius r as shown in Fig. 4.3 (a). The concentric path of vertical collector current can be seen and verified from 2-D device simulation (PISCES) as shown in Fig. 4.3 (b). The minimum radius r' is $(W_{bo}/m)+x_j$ where m is the only empirical constant. The maximum radius is $(W_{bo}/m)+x_j+W_{epi}$ as one can see in Fig. 4.3. Since the length of the curvature is $2r\theta$, the vertical geometric factor becomes

$$F_{GCV} = \frac{I_{ce}}{I_{co}} = \frac{p'_{nEV}}{p'_{nEL}} F'_{GCV}$$

$$\begin{aligned} F'_{GCV} &= a \int_{\frac{W_{bo}}{m}+x_j}^{\frac{W_{bo}}{m}+x_j+W_{epi}} \frac{dr}{2r\theta} = \frac{a}{2} \int_{sec^{-1}\left(1+\frac{W_{epi}}{x_j}+\frac{W_{bo}}{mx_j}\right)}^{sec^{-1}\left(1+\frac{W_{bo}}{mx_j}\right)} \frac{tan\theta}{\theta} d\theta \\ &= \frac{a}{2}\left[x + \frac{x^3}{9} + \frac{2x^5}{75} + \cdots\right]_{sec^{-1}\left(1+\frac{W_{bo}}{mx_j}\right)}^{sec^{-1}\left(1+\frac{W_{epi}}{x_j}+\frac{W_{bo}}{mx_j}\right)} \\ &= \frac{a}{2}\left[x + \frac{x^3}{9} + \frac{2x^5}{75} + \cdots\right]_{sec^{-1}\left(1+\frac{a}{m}\right)}^{sec^{-1}\left(1+\frac{a}{m}+u\right)} \end{aligned} \qquad (4.7)$$

where p'_{nEL} and p'_{nEV} represent the injected hole concentration at the lateral and vertical junction of the emitter, respectively, and m is a coefficient which is dependent on the geometry of the transistor. In general, m is 8.

Therefore, the vertical geometrical factor F_{GCV} is

$$F_{GCV} = F'_{GCV} \cdot exp\left(\frac{V_V - V_L}{V_t}\right) \qquad (4.8)$$

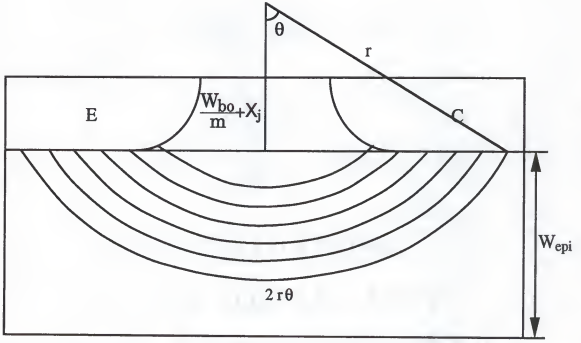


Figure 4.3 (a) The flow lines of vertical components of collector current originating under the emitter. This vertical current path is modeled by concentric curves.

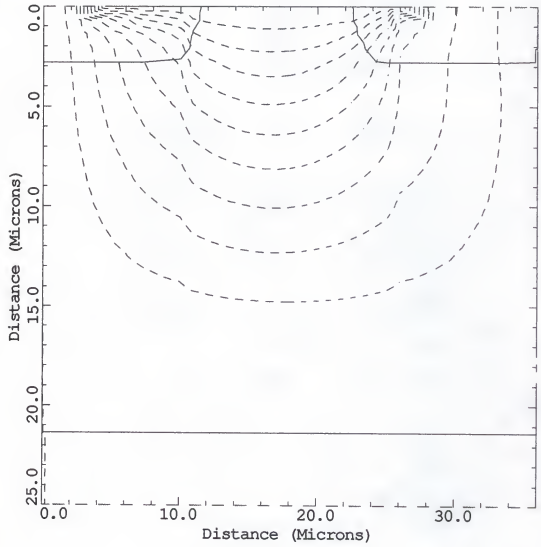


Figure 4.3 (b) The flow lines of collector current from PISCES simulation.

where V_V and V_L represent the voltage of the vertical junction and lateral junction, respectively.

4.2.3 Summary

The total F_{GC} is the sum of F_{GCL} and F_{GCV}. Fig. 4.4 compares the geometric factor with that of Chou [CHO71]. It can be seen that our analytical geometric factor can predict the 2-D effect within 5 % error range.

A complete analytical expression for the collector current for lateral pnp transistor is

$$I_C = I_{CO}\, F_{GC}\left(\frac{W_{bo}}{x_j} \cdot \frac{W_{epi}}{x_j}\right) \tag{4.9}$$

where $F_{GC} = F_{GCL} + F_{GCV}$.

4.3 Collector Current Modeling

4.3.1 One-Dimensional Collector Current

The differential equation for the hole current density is given by [GRA85]

$$J_p = qD_p\left(\frac{2p + N_D}{p + N_D}\frac{dp}{dx} + \frac{p}{p + N_D}\frac{dN_D}{dx}\right) \tag{4.10}$$

Since the doping concentration of base region N_D is uniform, the differential equation becomes

$$J_p = qD_p\left(\frac{2p + N_D}{p + N_D}\frac{dp}{dx}\right) \tag{4.11}$$

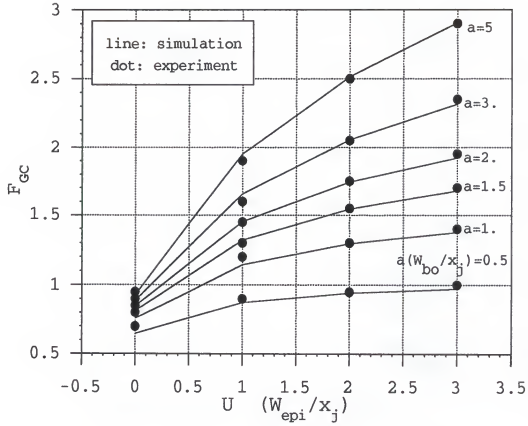


Figure 4.4 The geometrical factor, F_{GC}, is given as a function of u and a. The solid dots represent the experimental geometrical factor from [CHO71] and the solid lines show our analytical geometrical factor.

The solution of this differential equation is

$$J_p = -\frac{qD_p}{W_{bo}} \frac{2p_o + N_D}{p_o + N_D}(p_o - p_b)$$

$$where \quad p_o(p_o + N_D) = n_i^2 exp\left(\frac{V_{eb}}{V_t}\right) \qquad (4.12)$$

$$p_b(p_b + N_D) = n_i^2 exp\left(\frac{V_{bc}}{V_t}\right)$$

In the above equations, p_o and p_b are the excess minority carrier concentration at the base side of the emitter and collector junction space charge region, respectively, and V_t is kT/q. Then I_{co} becomes

$$I_{co} = J_p A_{EL} \qquad (4.13)$$

where $A_{EL} = l_e x_j$.

This one-dimensional current is valid at all injection-level conditions including high injection in the base region.

4.3.2 Emitter Resistances

Since the collector current is divided into two different components, a lateral current and a vertical current, the resistances of the current paths differ. R_{eL} is the resistance which the lateral current experience in the emitter region. It can be approximated by the resistance as seen from the endpoint of the metal contact to the junction sidewall, of which the length is L. It is given by [GRA77]

$$R_{eL} = \frac{L}{l_e}\left[\frac{1}{\int_0^{x_j} q\mu_n N_A(x)\,dx}\right] = \frac{L}{ql_e\overline{\mu_n}}\left[\frac{1}{\int_0^{x_j} N_A(x)\,dx}\right] \qquad (4.14)$$

R_{eV} is the resistance experienced by vertical current and can be calculated in the same way as R_{eL}

$$R_{eV} = \frac{x_j}{l_e} R_{eV} = \left(\frac{x_j}{l_e}\right)^2 \left[\frac{1}{\int_0^{x_j} q\mu_n N_A(x)\,dx}\right] \qquad (4.15)$$

In our case, L=5.4 μm, l_e=18 μm, x_j=2.8 μm and $N_A(x) = 10^{18}\,exp\left(-\frac{x}{\eta}\right)$ and η=0.405. The resultant R_{eL} is 160.74 Ω and R_{eV} is 12.96 Ω. Since R_{eL} is much larger than R_{eV}, the voltage of the emitter sidewall is smaller than that of emitter bottom, thus the vertical current component dominates at high current level. This is a form of emitter crowding.

4.3.3 Base Resistance

Base resistance has three components; the resistance (1) from base contact to buried layer, (2) of the buried layer, and (3) from the buried layer to the active device regions. This base resistance can be approximated in the same way as the collector resistance of vertical npns because they have a similar geometry. As the collector current increases, the component (3) undergoes conductivity modulation. Therefore, the resistance of component (3) is a function of current

$$R_{BI} = f\frac{\rho W_{epi}}{A} = f\frac{W_{epi}}{Apq\mu} = f\frac{W_{epi}^2}{\mu Q_V} \qquad (4.16)$$

where Q_V represents the total charge in the vertical transistor and f is a geometrical factor.

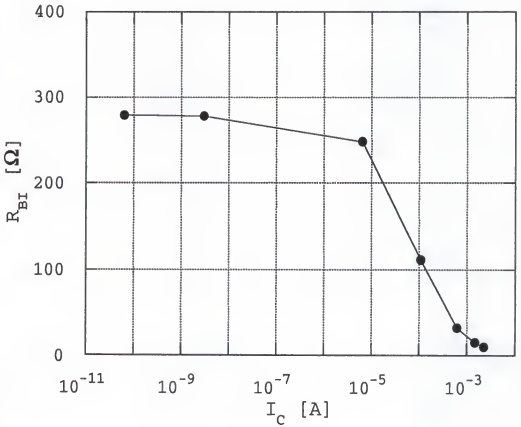


Figure 4.5 Base resistance of lateral pnp transistor as a function of collector current.

Fig. 4.5 shows the base resistance as a function of bias. It can be seen that the base resistance is a strong function of bias due to conductivity modulation in the base region.

4.4 Base Current Modeling

The base current has three major components:

(1) recombination in the neutral base (I_{B1}),

(2) back injection current in the neutral emitter (I_{B2}), and

(3) recombination in the emitter-base space-charge region (I_{B3}).

The current component for recombination in the neutral base is given by [CHO71]

$$I_{B1} = q \int_{base} \frac{p'(r)}{\tau_p} dV = \frac{q p'_{ne} V^*_B}{\tau_p} \tag{4.17}$$

where p'(r) is the excess hole concentration as a function of position and p'_{ne} is the excess hole concentration at the base edge of the emitter-base space charge region. Fig. 4.6 shows the 'effective volume' V^*_B depending on the geometry. Y_{re} is the y-coordinate of maximum radius of curvature at the bottom junction as shown in Fig. 4.6 and is calculated by

$$Y_{re} = \sqrt{\left(\frac{W_{bo}}{m} + x_j + W_{epi}\right)^2 - \left(\frac{W_{bo}}{m} + x_j\right)^2} \tag{4.18}$$

If Y_{re} is less than $l_e/2$, the 'effective volume' becomes

$$V^*_B = 2 * Area(Y_{re}) * l_e \tag{4.19}$$

or is same as 'effective volume' of [CHO71]. τ_p is typically 10^{-5} sec in low doped epitaxial silicon.

Electrons that are injected into the emitter recombine either in the bulk or the surface of the emitter surface. If the surface recombination dominates over the bulk recombination, the back injected current in the emitter is

$$I_{B2} = q\, n_i^2\, A_E \frac{D_{nE}}{Q_E} [\epsilon xp(qV_{EB}/kT) - 1] \qquad (4.20)$$

where Q_E is the total emitter doping concentration per unit area.

Recombination in the emitter-base space charge region is approximated by

$$I_{B3} = \frac{qn_iW}{2\tau_o} A_E \epsilon xp\left(\frac{qV_{EB}}{2kT}\right) \qquad (4.21)$$

where W is the width of space charge region and τ_o is the carrier lifetime in the space charge region and typically 10^{-4} sec.

In low injection, I_{B1} and I_{B3} are dominant but I_{B2} is dominant at high injection levels. Since our pnp device has a large base width, the recombination current in the neutral base region is an important component in low- to mid-injection conditions.

4.5 Substrate Transistor

The lateral pnp transistor has inherent parasitic pnp transistors associated with it, formed between the emitter or collector and p-type substrate. The n^+ buried layer blocks the current into the substrate, thereby reducing the leakage current to the substrate.

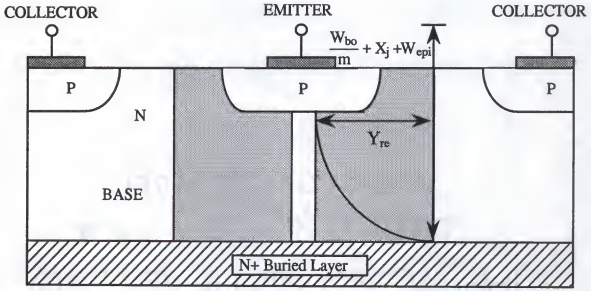


Figure 4.6 The shaded region represents effective base area for calculation of recombination current in the neutral base.

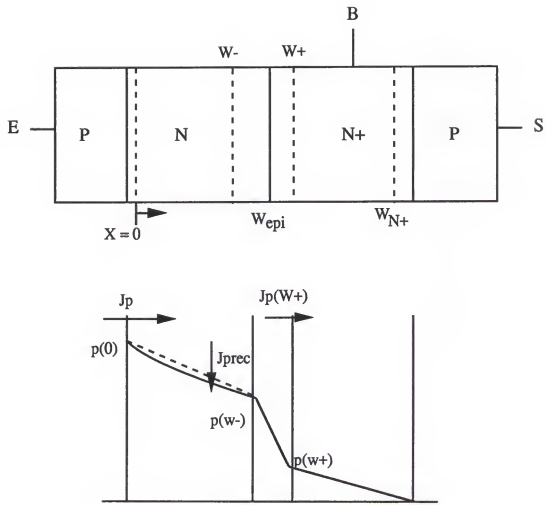


Figure 4.7 The one-dimensional p-n-n^+-p substrate transistor and the hole injection concentration into the base region.

Fig. 4.7 shows the injected carrier distribution in the base region (NN^+ region). The recombination current inside the high-low junction can be neglected and the recombination current in the N_{epi} region can be neglected since diffusion length L_p is much larger than epitaxial thickness in our case.

Since the recombination current inside the high-low junction is neglected, the current entering the high-low space-charge region ($J_p(W^+)$) is same as the one going out the space-charge region ($J_p(W^-)$). Thus,

$$J_p(W'^+) = \frac{qD_p^+ p(W'^+)}{W'_{N^+}} = \frac{qD_p\left[p(0) - p(W'^-)\right]}{W'_{epi}} = J_p(W'^-) \qquad (4.22)$$

If the diffusion length of the buried layer, L_p^+ is less than W_N^+, L_p^+ replaces W_N^+ in (4.22). The ratio of the hole concentrations on either side of the high-low junction becomes

$$\frac{p(W'^+)}{p(W'^-)} = \frac{N_D + p(W'^-)}{N_D^+} \qquad (4.23)$$

From (4.22) and (4.23), $p(W^-)$ can be evaluated as a function of $p(0)$, N_D and N_D^+. Therefore, the substrate current becomes

$$I_S = J_p(W'^-)\, A_{EI} \qquad (4.24)$$

4.6 Results and Discussion

Fig. 4.8 shows the Gummel plot (I_C, I_B and I_S vs V_{EB} for V_{BC} = 0V) of the lateral pnp transistor. I_S is the collector current of the substrate transistor. In Fig. 4.8, high injection in the base occurs at low bias (V_{EB} = 0.55 V) because of low doping in the base region and low current gain (β_{max} = 35) because of large base width. The simulations also show good agreement with measured data including substrate currents.

Fig. 4.9 is the flowchart for calculating the collector current depending on the emitter-base bias voltage given the collector-emitter voltage and base current. The model routine, given V_{CE} and I_B, first calculates the base current at an initial value of V_{EB}. Since the space-charge width of a junction depends on the junction voltage, the space-charge widths of emitter-base junction (W_{SE}) and collector-base junction (W_{SC}) are estimated at given bias conditions. W_{SC}, however, is also affected by collector current at high currents [Mul77]

$$W_{SC} = \frac{W_{SCO}}{\left(1 + \frac{I_C}{I_O}\right)^{1/2}} \tag{4.25}$$

where I_O represents the critical current dividing the low- and high-current regions. From these values of space-charge widths, the minimum base width, W_{bo}, and epitaxial thickness, W_{epi}, can be evaluated and, also, geometrical factors are calculated. The

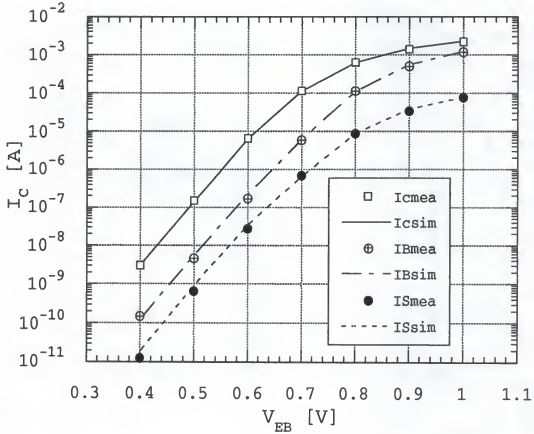


Figure 4.8 The forward active Gummel plot comparing the simulation with the measurement.

internal voltages, V_{EBL} and V_{EBV}, are calculated by

$$V_{EBL} = V_{EB} - R_{EL} * I_{EL} - R_B * I_{BL}$$
$$V_{EBV} = V_{EB} - R_{EL} * I_{EV} - R_B * I_{BV} \qquad (4.26)$$

The base current can be computed using these internal voltages. The routine iterates to find a correct V_{EB} which satisfies the calculated base current is same as the given base current. Using calculated values for F_{GCL}, F_{GCV}, V_{EBL} and V_{EBV}, the collector current becomes

$$I_C = I_{CO}\left(F_{GCL} + F'_{GCV}\ exp\left(\frac{V_{EBV} - V_{EBL}}{V_t}\right)\right) \qquad (4.27)$$

To model the transistor in both the forward-active and saturation modes, the geometrical factors are generalized. A current flows from collector to emitter for forward-biased collector-base junction. The total current in saturation mode can be estimated by the superposition of currents between emitter and collecter. Therefore, the geometrical factor is modified to

$$F_{MGCL} = \frac{I_{CL} - I_{RL}}{I_{CO}} = \frac{I_{CL} - I_{RL}}{I_{CL}} \frac{I_{CL}}{I_{CO}} \qquad (4.28)$$

where I_{RL} represents the lateral current from collector to emitter. Using above equation, the generalized geometrical factors are

$$F_{MGCL} = \frac{p_o A_{EL} - p_b A_{CL}}{p_o A_{EL}} F_{GCL}$$
$$F_{MGCV} = \frac{p_o A_{EV} - p_b A_{CV}}{p_o A_{EV}} F_{GCV} \qquad (4.29)$$

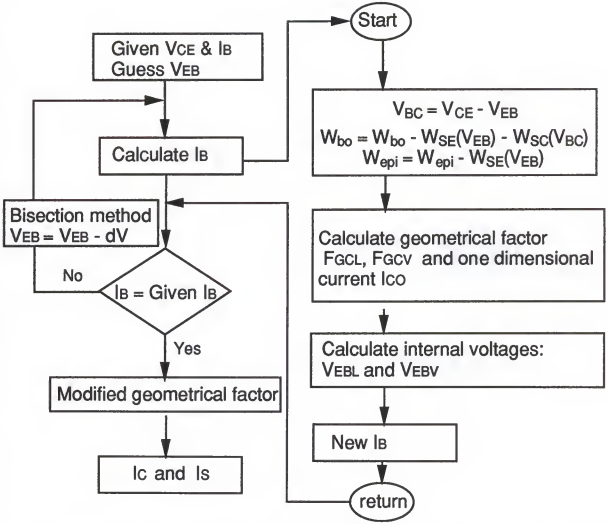


Figure 4.9 The flowchart for calculating collector current as a function of emitter-base junction voltage with given collector-emitter voltage and base current.

where A_{EL} and A_{CL} is the sidewall area of the emitter and collector, respectively, and A_{EV} and A_{CV} is the bottom area of the emitter and collector, respectively. Fig. 4.10 shows the I_C vs. V_{CE} using these modified geometrical factor. The simulations in this figure show excellent agreement with the measured data in the saturation and the active regions. This analytical model can predict the collector current of the lateral pnp transistor very accurately at all injection conditions.

4.7 The Transient Modeling of Lateral PNP Transistor

4.7.1 Simulation

Fig. 4.11 shows the large-signal model of the lateral pnp transistor. This charge-based model simulates the charging current

$$\frac{dQ_i}{dt} = \sum_j \frac{\partial Q_i}{\partial V_j} \frac{dV_j}{dt} \tag{4.30}$$

where i, j = BEL, BEV, BCL and BCV. The charge dynamics are based on the quasi-static approximation with the regional charges.

Fig. 4.12 shows the regional charges in the lateral pnp transistor. The subscripts L and V represent the lateral transistor and vertical transistor, respectively. Using the Gummel-Poon equation, the total charge in the base region of

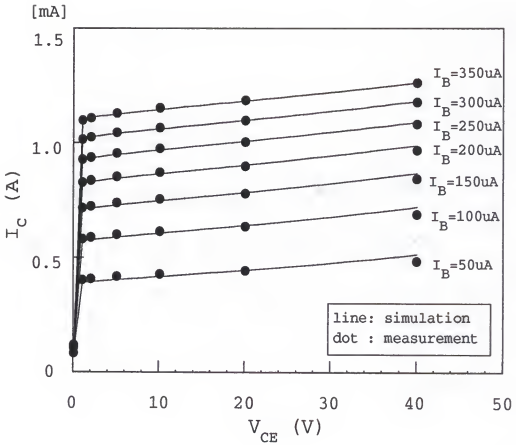


Figure 4.10 The collector current as a function of collector-emitter voltage for different base current levels.

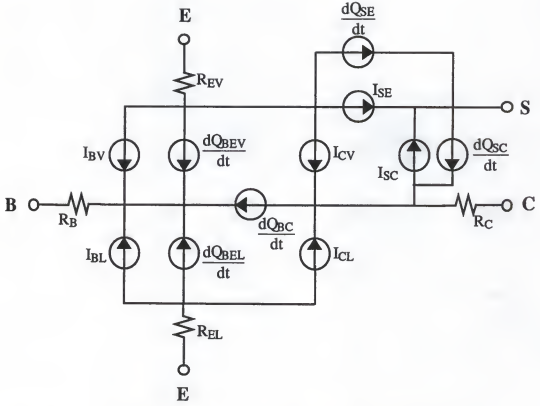


Figure 4.11 Complete network representation of the charge-based lateral pnp transistor model.

lateral the transistor is

$$
\begin{aligned}
Q_{BBL} &= ql\int_0^{x_j}\left[\int_{x_E(x)}^{x_C(x)} p\,dy\right]dx + ql\int_0^{x_j}\left[\int_0^{W_{BM}(x)} N_D\,dy\right]dx \\
&\quad - ql\int_0^{x_j}\left[\int_{x_C(x)}^{W_{BM}(x)} N_D\,dy\right]dx - ql\int_0^{x_j}\left[\int_0^{x_E(x)} N_D\,dy\right]dx \\
&= q_A l\frac{q\overline{D_p}n_i^2 A_l}{I_{cl}}\left[\epsilon xp\left(\frac{V_{EBL}}{V_t}\right) - \epsilon xp\left(\frac{V_{BC}}{V_t}\right)\right] \\
&\equiv Q_{NL} + Q_{BOL} + Q_{JEL} + Q_{JCL}
\end{aligned}
\tag{4.31}
$$

Since the doping density of base region is uniform, the integrals become

$$
\begin{aligned}
Q_{BOL} &= ql\int_0^{x_j} N_D W_{BM}(x)\,dx \\
Q_{JEL} &= -ql\int_0^{x_j} N_D x_E(x)\,dx = -q\frac{\pi}{2}(lx_j)N_D x_E(0) \\
Q_{JCL} &= -ql\int_0^{x_j} N_D[W_{BM}(x) - x_C(x)]dx \\
&= -\frac{q\pi}{2}(lx_j)N_D[W_{BM}(0) - x_C(0)]
\end{aligned}
\tag{4.32}
$$

where W_{BM} represents the distance to collector-base metallurgical junction.

The injected charge in the lateral transistor base region can be calculated from (4.32). Since the injected charge is a function of collector current, the injected charge in the vertical transistor base region, Q_{NV}, is

$$
Q_{NV} = \frac{I_{CV}}{I_{CL}} Q_{NL} \tag{4.33}
$$

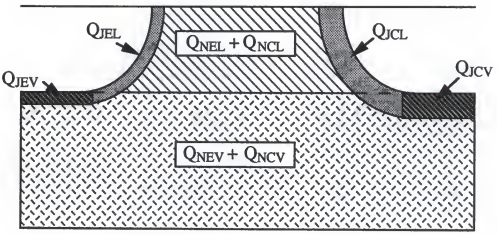


Figure 4.12 The regional charges of lateral pnp transistor.

Using the partition-charge (PC) method [FOS86] which accounts for the NQS delay to the first order, the injected charge can be divided as

$$Q_{NL} = Q_{NL}^{E} + Q_{NL}^{C} = Q_{NL} f_B + Q_{NL}(1 - f_B)$$
$$Q_{NV} = Q_{NV}^{E} + Q_{NV}^{C} = Q_{NV} f_B + Q_{NV}(1 - f_B) \qquad (4.34)$$

Finally, the total charges corresponding to each junction bias are

$$Q_{BEL} = Q_{EEL} + f_B Q_{NL} - Q_{JEL}$$
$$Q_{BEV} = Q_{EEV} + f_B Q_{NV} - Q_{JEV} \qquad (4.35)$$
$$Q_{BCL} = (1 - f_B) Q_{NL} + Q_{JCL} \qquad Q_{BCV} = (1 - f_B) Q_{NV} + Q_{JCV}$$

where Q_{EEL} and Q_{EEV} represent the injected charges in the emitter.

4.7.2 Measurement

The transistor is measured under active turn-on and turn-off cases for $V_{EC} = -2$ V and the base is driven with a voltage source which ramps at a rate 7 mV/ns from 0 to 0.7 V, then remains at 0.7 V.

4.7.3 Results and Discussion

Since this lateral pnp transistor has a wide base, NQS delay can be a great factor in transient and ac modeling. We adopt the PC method to account the NQS effects. Since the transient measurement for lateral pnp transistor is somewhat easier than for the npn transistor, this can be a good case to verify the PC model. The charge partitioning factor f_B is taken as 0.7 for our

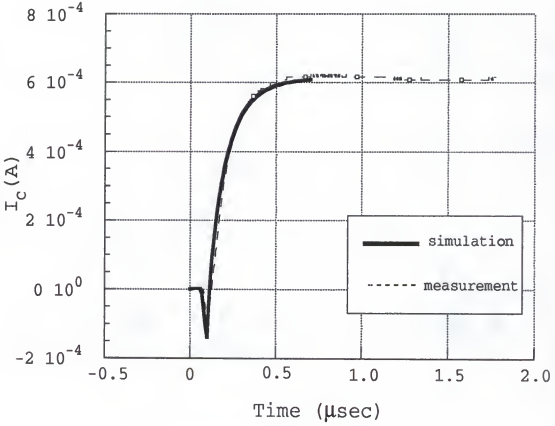


Figure 4.13 (a) Transient simulation and experimental data for turn-on case. The transient time of input step voltage is 0.1 μsec.

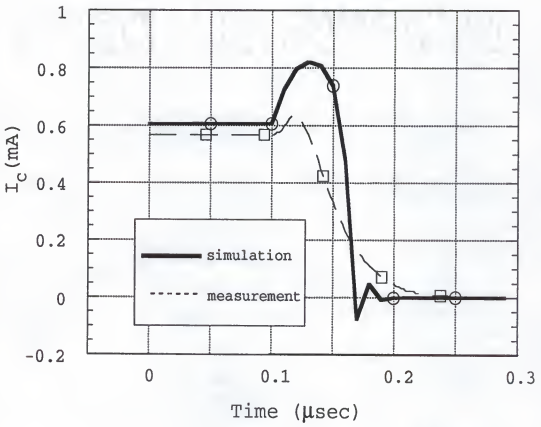


Figure 4.13 (b) Transient simulation and experimental data for turn-off.

simulation. Fig. 4.13 shows the turn-on and turn-off transient simulation and measured data. The simulation shows excellent agreement with the measurements in the turn-on case and thus, the PC model is sufficient for our case without a complex equation for NQS effect. The rise time of the lateral pnp transistor is about 0.4 μs. After 0.5 μs, I_C remains at 0.6 mA, which is consistent with the dc value. For this simulation, our model is put into SPICE. The implementation to the SPICE is shown in Appendix.

4.8 The Small-Signal Modeling of Lateral PNP Transistor

4.8.1 Simulation

There are several approaches for developing a small-signal model [WHI70, KRO75, REI87]. The approach adopted here directly determines the small-signal model elements from the large-signal model at a given bias. The small-signal elements are evaluated as the derivatives of each current source in the large-signal charge-based model about its current-source control voltage. By rearranging these derivatives, the linearized elements of the small-signal model can be derived. The charges and currents depend on the independent variable V_{EBL}, V_{EBL}, V_{EBL} and V_{EBL} and the derivatives of these terms become capacitances, resistances, transcapacitances and transconductances. Table 4.1 shows the derivation of the small-signal elements.

Table 4.1 Small-signal model circuit elements.

$C_{\pi l} = \frac{\partial Q_{BEL}}{\partial V_{BEL}} + \frac{\partial Q_{BCL}}{\partial V_{BEL}}$	$C_{\pi v} = \frac{\partial Q_{BEV}}{\partial V_{BEV}} + \frac{\partial Q_{BCV}}{\partial V_{BEV}}$
$C_{\mu l} = \frac{\partial Q_{BEL}}{\partial V_{BCL}} + \frac{\partial Q_{BCL}}{\partial V_{BCL}}$	$C_{\mu v} = \frac{\partial Q_{BEV}}{\partial V_{BCV}} + \frac{\partial Q_{BCV}}{\partial V_{BCV}}$
$g_{\pi l} = \frac{\partial I_{BL}}{\partial V_{BEL}}$	$g_{\pi V} = \frac{\partial I_{BV}}{\partial V_{BEV}}$
$g_{ol} = -\frac{\partial I_{CL}}{\partial V_{BC}} - \frac{\partial I_{BL}}{\partial V_{BCL}}$	$g_{ov} = -\frac{\partial I_{CV}}{\partial V_{BC}} - \frac{\partial I_{BV}}{\partial V_{BCV}}$
$g_{ml} = \frac{\partial I_{CL}}{\partial V_{BEL}} + \frac{\partial I_{BL}}{\partial V_{BCL}}$	$g_{mv} = \frac{\partial I_{CV}}{\partial V_{BEV}} + \frac{\partial I_{BV}}{\partial V_{BCV}}$

Fig. 4.14 shows the small-signal equivalent circuit model of the lateral pnp transistor of which the elements are taken from Table 4.1 where l and v represent the lateral and the vertical transistor, respectively.

4.8.2 Measurement

The input and output y-parameters (y_{11} and y_{22}) can be measured directly using HP 4194 Impedance Analyzer. Since this analyzer

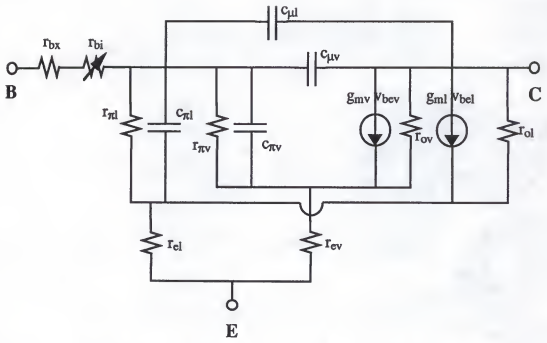


Figure 4.14 The small-signal equivalent circuit of lateral pnp transistor.

supports only single-port measurements, it was necessary to design a circuit to perform the 2-port y-parameter measurements.

The schematic of the circuit for measuring y_{21} is shown in Fig. 4.15. R_1 should be much higher than the input impedance of the transistor. Since R_1 and R_2 set the dc bias of the emitter-base and emitter-collector junctions, respectively, the choice of resistor value is critical for the wide range of bias measurement. C_1 and C_2 are blocking capacitors. To measure the short-circuit output current, R_{out} should be as small as possible but large enough to detect the output voltage. Also R_{out} should be much smaller than R_2 so that the majority of the output small-signal current passes R_{out}.

4.8.3 Results and discussion

Fig. 4.16 shows the simulated unity-gain frequency (f_T) as a function of current (I_C). One can see that the unity-gain frequency is much lower than for typical npn transistors (~ 10 GHz). The lateral pnp transistor can be a major source of delay in integrated circuits. Also, the unity-gain frequency is saturated above $V_{EB} = 0.65$. Since our lateral transistor has no epitaxial collector region, which modern npn transistors generally have, base widening is limited to inside the metallurgical base width. Since base transit time is a dominant delay in the high-current region [ROU86], the unity-gain frequency is saturated.

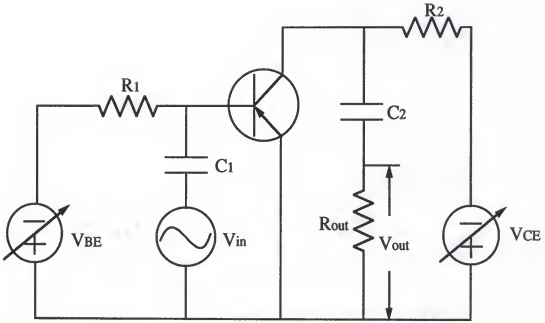


Figure 4.15 The schematic of the circuit for measuring the y_{21} parameter.

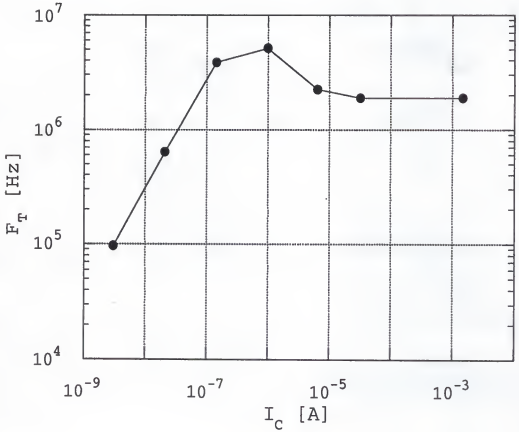


Figure 4.16 The cutoff frequency (f_T) as a function of collector current.

Fig. 4.17 shows the simulated y-parameters of a lateral transistor compared to measured data. These figures show excellent agreements between model and measurements in both magnitude and phase. Fig. 4.17 (a) and (b) shows the magnitude and phase of y_{11}. In Fig. 4.17(b), there is a slight difference at high frequencies. Since we are using chips for the measurement, the parastics of the chip can affect the measurement in the high frequency region. Fig. 4.17 (c) and (d) shows the y_{22} magnitude and phase. Generally speaking, it is difficult to simulate y_{22} exactly because there are many parastics at the output port and it is difficult to predict the dominant one. However, this lateral pnp transistor model shows a good agreement with measurement. Fig. 4.17 (e) shows the y_{21} magnitude. Since h_{21} is y_{21}/y_{11}, we can see the cutoff frequency is about 2 MHz and the down slope is about 20 dB/decade from Fig. 4.17 (a) and 4.17 (e).

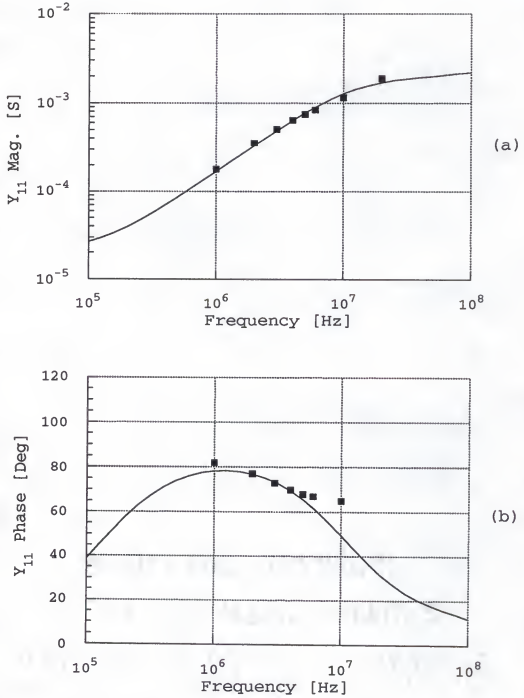


Figure 4.17 (a) A comparison of the magnitude and (b) the phase of the simulated y_{11} with measured data.

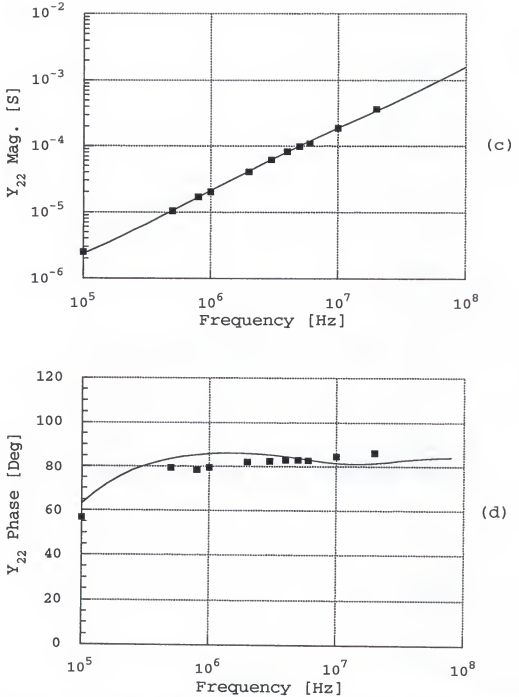


Figure 4.17 (c) A comparison of the magnitude and (d) the phase of the simulated y_{22} with measured data.

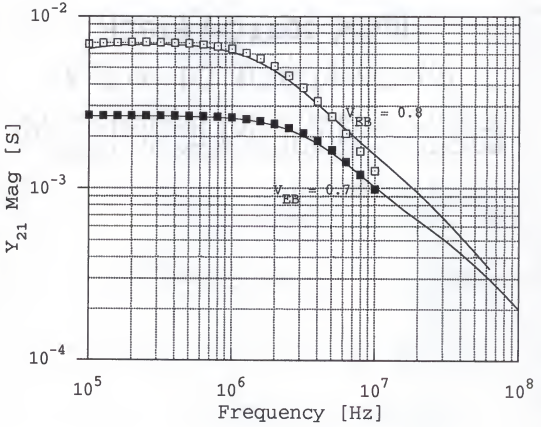


Figure 4.17 (e) A comparison of the magnitude of the simulated y_{21} with measured data.

CHAPTER 5
SUMMARY AND SUGGESTIONS

In this dissertation, procedures for measuring the small-signal BJT response and models for active and passive elements in BJTs have been developed and verified with measurements. A new de-embedding method called three-step de-embedding method is developed to correct the environment of the device-under-test (DUT) from the s-parameter measurement. In this de-embedding method, the correction includes the series parastics as well as the shunting parastics of the pads and interconnects. Using this corrected measurement data, the base impedance of advanced BJTs, which includes the dc and ac crowding effect in the emitter-base junction can be extracted. The method for extracting the base impedance equivalent circuit elements is derived from the general hybrid-π equivalent circuit (including C_{μ}). From the measurements of base impedance, an intrinsic base small-signal capacitance is extracted which is frequency independent, but bias dependent. The importance of this extracted capacitance is that it is not predicted in the existing charge-based model. It is left for future work to model this capacitance and incorporate it into the charge based model.

A very physical charge-based model for the lateral pnp transistor is developed for predictive simulation of dc, ac and

transient operation. This analytical model simplifies the two-dimensional current flow by deriving the analytical geometrical factors for the two predominant collector current components of the lateral device. Substrate p-n-n^+—p transistor which is a parastic transistor is also modeled and incorporated into the lateral pnp BJT model. This model shows great accuracy in predicting the dc, ac and transient behavior of the lateral pnp transistor. This fully developed lateral pnp transistor model is implemented in mixed-mode SPICE.

Based on the completed research discussed herein, we suggest the following subjects for future research consideration.

First, we recommend the physical modeling of non-quasi-static effects in the base region of the lateral pnp transistor. Since this lateral pnp transistor has a wide base-width generally, these NQS effects can be important in the resulting circuit design using the lateral pnp transistor. Since the charge partitioning method, which takes care of this NQS effect in the first order, is used for developing the transient and small-signal models from the charge calculated from the dc solution, the physical modeling of the partitioning factor can be consistent with charge-based model.

Second, we recommend the investigation of the generality of our lateral pnp model for a wide range of variations in layout geometry. Our model is scalable and suitable for the geometry which the emitter is completely surrounded by the collector.

But in the bipolar VLSI circuits, there are lots of variation in geometry (for example, the collector is a strip-line parallel to the emitter in the I^2L circuit). Also there can be many variation in the geometry inside the device (lateral n-p-n transistor in the CMOS device).

Third, we suggest that the lateral pnp transistor is a vehicle for studying the temperature-dependences of carrier transport in p^+ regions. These measurements can be used to choose between different models at the device simulator level by comparing measurement with simulation.

Fourth, we recommend the physical modeling of the intrinsic base capacitance. The characterization of base impedance is crucial in small-signal modeling. We have developed methods to extract base impedance from s-parameter measurement. This can be a basis for developing and verifying the model for base impedance.

Fifth, based on the work herein and previous modeling efforts of others, we recommend that the large-signal models for the vertical and lateral BJT be further verified against large-signal measurements. This can be done with existing equipment and is critical to promoting the relevancy of the charge-based modeling approach. There are still many distributed and/or nonquasistatic effects which have probably not been modeled extensively.

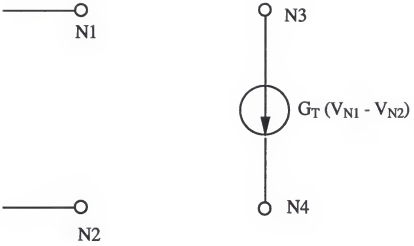
APPENDIX
THE IMPLEMENTATION OF THE LATERAL PNP BJT MODEL IN MMSPICE

1. Introduction

The physical charge-based lateral bipolar junction transistor (BJT) model has been implemented in MMSPICE, a mixed-mode device/circuit simulator developed at the University of Florida. Since the lateral BJT model has four internal nodes (npn BJT model has 3 internal nodes), this appendix can be helpful for implementation of future model into SPICE. Section 2 explains the general procedure to build the admittance matrix. Section 3 shows the procedure of implementing the model into the SPICE. In this section, the variables of the QLBJT (this routine calculate the derivatives of the regional charge) and QLBCT (the model routine) are shown.

2. Admittance Matrix

The equivalent nodal admittance matrix of the single voltage-controlled current source is shown in Fig. A.1 [Mcc88]. By applying this method to the large-signal model of the lateral BJT in Fig. A.2, the admittance matrix can be evaluated as shown in Table A.1.



	N1	N2	N3	N4
N1				
N2				
N3	G_T	$-G_T$		
N4	$-G_T$	G_T		

Figure A.1 The equivalent nodal admittance matrix of the single voltage-controlled current source.

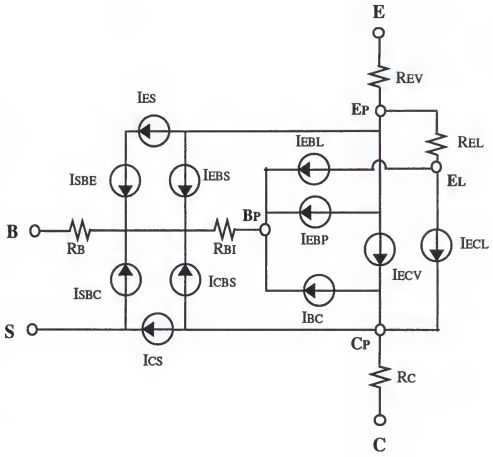


Figure A.2 Complete large-signal model of the lateral BJT.

3. Model Implementation into SPICE

The first step to implement the model into MMSPICE is to find the available ID number from the routine find.f. In this case, 16 and 26 are the ID numbers for the QLBJT and QLBCT, respectively. The next step is to build the variable list of the each routine. The Table A.2, A.3 and A.4 show the variable list of the QLBJT and QLBCT respectively. Generally, there are two kinds of variable in SPICE, one is the integer variable and the other is the real variable. To build the integer variable list, the non-zero elements in the admittance matrix is used. The state variable (Lxi) include the junction voltage, current and the derivatives of charges and currents. The variable list of the QLBCT is the input parameters of the model as shown in Table A.3. The default value, the nominal value and the unit of the input parameters are shown in Table A.5.

The details of changing other routines are shown in MMSPICE programmer's reference manual.

Table A.1 Admittance matrix of the lateral pnp transistor

	C	B	E	S	CP	BP	EP	EL
C	$\frac{1}{R_C}$				$-\frac{1}{R_C}$			
B		$\frac{1}{R_B} - \frac{\partial I_{SBC}}{\partial V_{BCP}} - \frac{\partial I_{SBC}}{\partial V_{BS}} - \frac{\partial I_{CBS}}{\partial V_{BS}} - \frac{\partial I_{CBS}}{\partial V_{BCP}} - \frac{\partial I_{EBS}}{\partial V_{BS}} - \frac{\partial I_{EBS}}{\partial V_{BEP}} - \frac{\partial I_{SBE}}{\partial V_{BS}} - \frac{\partial I_{SBE}}{\partial V_{BEP}}$		$\frac{\partial I_{SBC}}{\partial V_{BS}} + \frac{\partial I_{CBS}}{\partial V_{BS}} + \frac{\partial I_{EBS}}{\partial V_{BS}} + \frac{\partial I_{SBE}}{\partial V_{BS}}$	$\frac{\partial I_{SBC}}{\partial V_{BCP}} + \frac{\partial I_{CBS}}{\partial V_{BCP}}$	$-\frac{1}{R_B}$	$-\frac{\partial I_{EBS}}{\partial V_{EPB}} - \frac{\partial I_{SBE}}{\partial V_{EPB}}$	
E			$\frac{1}{R_E}$				$-\frac{1}{R_E}$	

Table A.1 (Continued) Admittance matrix of the lateral pnp transistor

	C	B	E	S	CP	BP	EP	EL
S		$\frac{\partial I_{SBC}}{\partial V_{BCP}} + \frac{\partial I_{SBC}}{\partial V_{BS}} - \frac{\partial I_{SBE}}{\partial V_{EPB}} + \frac{\partial I_{SBE}}{\partial V_{BS}} + \frac{\partial I_{CS}}{\partial V_{BCP}} - \frac{\partial I_{CS}}{\partial V_{BS}} - \frac{\partial I_{ES}}{\partial V_{BS}} + \frac{\partial I_{ES}}{\partial V_{EPB}}$		$-\frac{\partial I_{SBC}}{\partial V_{BS}} - \frac{\partial I_{SBE}}{\partial V_{BS}} + \frac{\partial I_{ES}}{\partial V_{BS}} + \frac{\partial I_{CS}}{\partial V_{BS}}$	$-\frac{\partial I_{SBC}}{\partial V_{BCP}} + \frac{\partial I_{CS}}{\partial V_{BCP}}$		$-\frac{\partial I_{ES}}{\partial V_{EPB}} + \frac{\partial I_{SBE}}{\partial V_{EPB}}$	
CP	$-\frac{1}{R_c}$	$\frac{\partial I_{CBS}}{\partial V_{BS}} + \frac{\partial I_{CBS}}{\partial V_{BCP}} + \frac{\partial I_{CS}}{\partial V_{BS}} + \frac{\partial I_{CS}}{\partial V_{BCP}}$		$-\frac{\partial I_{CBS}}{\partial V_{BS}} - \frac{\partial I_{CS}}{\partial V_{BS}}$	$\frac{1}{R_c} - \frac{\partial I_{CBS}}{\partial V_{BCP}} + \frac{\partial I_{CS}}{\partial V_{CPB}} - \frac{\partial I_{ECL}}{\partial V_{CPBP}} + \frac{\partial I_{BCP}}{\partial V_{CPBP}} - \frac{\partial I_{ECV}}{\partial V_{CPBP}}$	$-\frac{\partial I_{BCP}}{\partial V_{EPBP}} + \frac{\partial I_{BCP}}{\partial V_{BPCP}} + \frac{\partial I_{ECV}}{\partial V_{EPBP}} - \frac{\partial I_{ECV}}{\partial V_{BPCP}} + \frac{\partial I_{ECL}}{\partial V_{ELBP}} - \frac{\partial I_{ECL}}{\partial V_{BPCP}}$	$\frac{\partial I_{BCP}}{\partial V_{EPBP}} - \frac{\partial I_{ECV}}{\partial V_{EPBP}}$	$-\frac{\partial I_{ECL}}{\partial V_{ELBP}}$

Table A.1 (Continued) Admittance matrix of the lateral pnp transistor

	C	B	E	S	CP	BP	EP	EL
BP		$-\frac{1}{R_B}$			$\frac{\partial I_{EBP}}{\partial V_{B_PC_P}} + \frac{\partial I_{BCP}}{\partial V_{B_PC_P}} + \frac{\partial I_{EBL}}{\partial V_{B_PC_P}}$	$\frac{1}{R_B} + \frac{\partial I_{EBP}}{\partial V_{E_PB_P}} + \frac{\partial I_{EBP}}{\partial V_{C_PB_P}} + \frac{\partial I_{BCP}}{\partial V_{E_PB_P}} + \frac{\partial I_{BCP}}{\partial V_{C_PB_P}} + \frac{\partial I_{EBL}}{\partial V_{E_LB_P}} + \frac{\partial I_{EBL}}{\partial V_{C_PB_P}}$	$-\frac{\partial I_{BCP}}{\partial V_{E_PB_P}} - \frac{\partial I_{EBP}}{\partial V_{E_PB_P}}$	$-\frac{\partial I_{EBL}}{\partial V_{E_LB_P}}$

Table A.1 (Continued) Admittance matrix of the lateral pnp transistor

	C	B	E	S	CP	BP	EP	EL
E P		$\frac{\partial I_{ES}}{\partial V_{BS}} - \frac{\partial I_{ES}}{\partial V_{E_PB}}$	$-\frac{1}{R_E}$	$-\frac{\partial I_{ES}}{\partial V_{BS}}$	$-\frac{\partial I_{EBP}}{\partial V_{B_PC_P}}$ $-\frac{\partial I_{ECV}}{\partial V_{B_PC_P}}$	$-\frac{\partial I_{EBP}}{\partial V_{E_PB_P}} + \frac{\partial I_{EBP}}{\partial V_{B_PC_P}}$ $-\frac{\partial I_{ECV}}{\partial V_{E_PB_P}} + \frac{\partial I_{ECV}}{\partial V_{B_PC_P}}$	$\frac{1}{R_E} + \frac{1}{R_{EL}}$ $+\frac{\partial I_{EBP}}{\partial V_{E_PB_P}}$ $+\frac{\partial I_{ECV}}{\partial V_{E_PB_P}}$ $+\frac{\partial I_{ES}}{\partial V_{E_PB}}$	$-\frac{1}{R_{EL}}$
E L		$\frac{\partial I_{EBS}}{\partial V_{BS}} - \frac{\partial I_{EBS}}{\partial V_{E_LB}}$		$-\frac{\partial I_{EBS}}{\partial V_{BS}}$	$-\frac{\partial I_{EBL}}{\partial V_{B_PC_P}}$ $-\frac{\partial I_{ECL}}{\partial V_{B_PC_P}}$	$-\frac{\partial I_{EBL}}{\partial V_{E_LB_P}} + \frac{\partial I_{EBL}}{\partial V_{B_PC_P}}$ $-\frac{\partial I_{ECL}}{\partial V_{E_LB_P}} + \frac{\partial I_{ECL}}{\partial V_{B_PC_P}}$	$\frac{\partial I_{EBS}}{\partial V_{E_PB}}$ $-\frac{1}{R_{EL}}$	$\frac{1}{R_{EL}}$ $+\frac{\partial I_{EBL}}{\partial V_{E_LB_P}}$ $+\frac{\partial I_{ECL}}{\partial V_{E_LB_P}}$

Table A.2 Integer variables of lateral pnp transistor(ID=16)

LOC+00:	next pointer	+22:	(nb',nc')
+01:	LOCV	+23:	(nb',ne')
+02:	nc	+24:	(nb',nel)
+03:	nb	+25:	(ne',nb)
+04:	ne	+26:	(ne',ne)
+05:	ns	+27:	(ne',ns)
+06:	nc'	+28:	(ne',nc')
+07:	nb'	+29:	(ne',nb')
+08:	ne'	+30:	(ne',nel)
+09:	nel	+31:	(nel,nc')
+10:	model pointer	+32:	(nel,nb')
+11:	off	+33:	(nel,ne')
+12:	(nc,nc')	+34:	Lxi offset
+13:	(nb,nb')	+35:	(nc,nc)
+14:	(ne,ne')	+36:	(nb,nb)
+15:	(ns,nb)	+37:	(ne,ne)
+16:	(ns,ne')	+38:	(ns,ns)
+17:	(nc',nc)	+39:	(nc',nc')
+18:	(nc',nb')	+40:	(nb',nb')
+19:	(nc',ne')	+41:	(ne',ne')
+20:	(nc',nel)	+42:	(nel,nel)
+21:	(nb',nb)		

Table A.3 Real variables of the lateral pnp transistor(ID=16)

LOCV		**Lxi**	
+00:	device name	+00:	vbe
+01:	AE	+01:	vbel
+02:	AC	+02:	vbc
+03:	XJ	+03:	ctl
+04:	WE	+04:	ctv
+05:	IC-Vbe	+05:	gctbel
+06:	IC-Vce	+06:	gctbev
+07:	RBI	+07:	gctbcl
		+08:	gctbcv
		+09:	cbl
		+10:	cbv
		+11:	gcbbel
		+12:	gcbbev
		+13:	gcbbcl
		+14:	gcbbcv
		+15:	qbel
		+16:	i(qbel)
		+17:	qbev
		+18:	i(qbev)
		+19:	qbcl
		+20:	i(qbcl)
		+21:	qbcv
		+22:	i(qbcv)
		+23:	cqbelbe
		+24:	cqbevbe
		+25:	cqbelbc
		+26:	cqbevbc
		+27:	cqbclbe
		+28:	cqbcvbe
		+29:	cqbclbc
		+30:	cqbcvbc
		+31:	gx
		+32:	vsub
		+33:	cts
		+34:	gctsbe
		+35:	gctsbs

Table A.4 Variables of the lateral pnp transistor model(ID=26)

LOC+00:	next pointer
+01:	LOCV
+02:	model type

LOCV+00:	model name
+01:	NEPI
+02:	WBM
+03:	WEPI
+04:	WBUR
+05:	NBUR
+06:	JEO
+07:	JSEO
+08:	NEB
+09:	WSEO
+10:	PE
+11:	ME
+12:	PC
+13:	DPB
+14:	PS
+15:	WSSO
+16:	DPBUR
+17:	TB
+18:	TO
+19:	RC
+20:	RBX
+21:	REV
+22:	REL
+23:	FBL
+24:	FBV

Table A.5 Input parameter of the lateral pnp transistor model.

NAME	DESCRIPTION	UNITS	DEF	TYPICAL
NEPI	Base doping density	cm^{-3}	1.E15	1.E15
WBM	Base width	m	1.E-5	1.E-5
WEPI	Epitaxial thickness	m	1.E-5	1.E-5
WBUR	Buried layer thickness	m	5.E-6	5.E-6
NBUR	Peak doping of buried layer	cm^{-3}	1.E18	1.E18
JEO	Emitter saturation current density	A. m^{-2}	1.E-8	1.E-8
JSEO	B-E SCR saturation current density	A. m^{-2}	1.E-4	1.E-4
NEB	B-E SCR emission coefficient	-	2.0	2.0
WSEO	B-E equilibrium SCR width	m	1.E-6	1.E-6
PE	B-E junction potential	V	1.0	1.0
ME	B-E junction exponential factor	-	0.4	0.4
PC	B-C junction potential	V	1.0	1.0
DPB	Effective hole diffusivity in base	cm^2s^{-1}	7.0	7.0
DPBUR	Effective hole diffusivity in buried layer	cm^2s^{-1}	4.0	4.0
TB	Carrier life time in base	s	1.E-6	1.E-6
TO	Carrier life time in SCR	s	1.E-5	1.E-5
RC	Extrinsic collector resistance	Ω	0	10
RBX	Extrinsic base resistance	Ω	0	50
REV	Extrinsic emitter resistance	Ω	0	10
REL	Lateral emitter resistance	Ω	0	100
FBL	Lateral charge partition factor	-	0.5	0.5
FBV	Vertical charge partition factor	-	0.5	0.5

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